Side-Channel Security

Chapter 3: Reverse Engineering Intel Last-Level Cache Mapping + AMD Way Predictor

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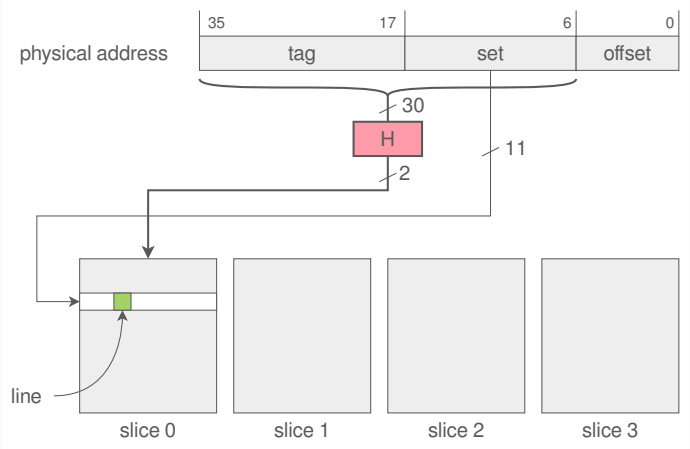
Last-level cache addressing



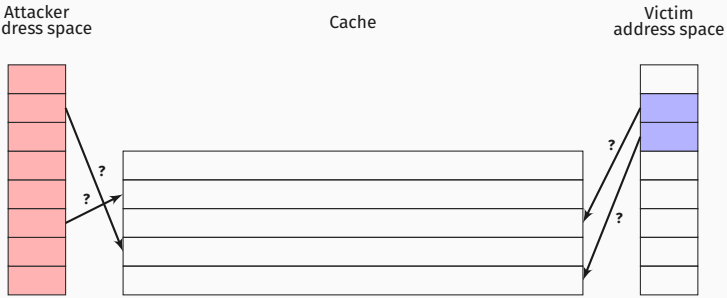
Last-level cache addressing

- last-level cache $\rightarrow$ as many slices as cores
- *undocumented* hash function that maps a physical address to a slice
- designed for performance

For 2^k slices:

Prime+Probe on recent procesors?

Complex addressing $\rightarrow$ impossible to *target a set*



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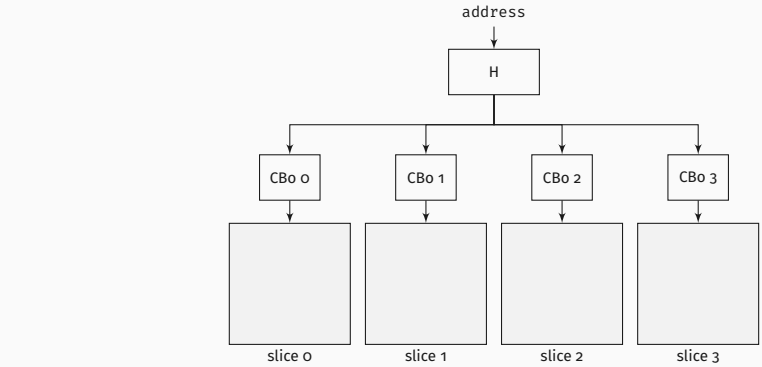

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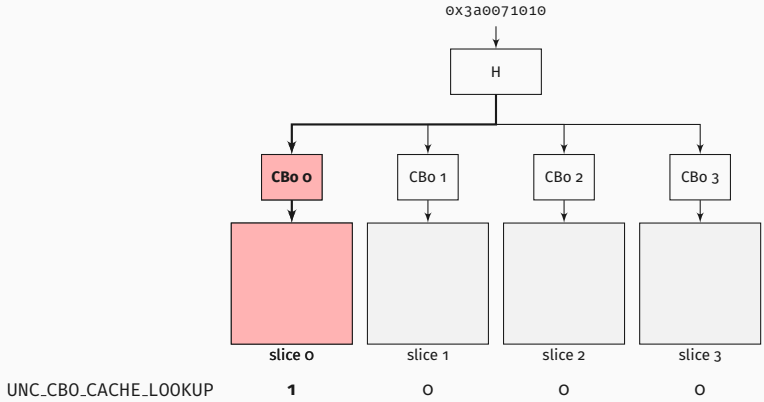

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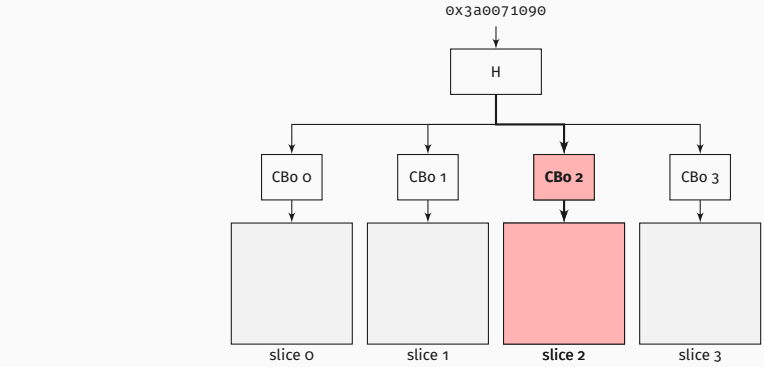

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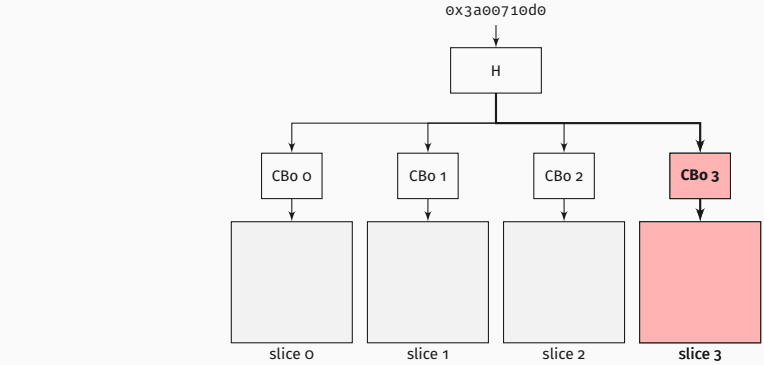

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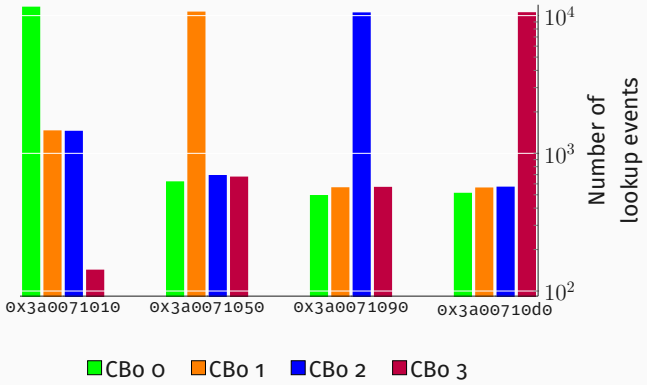
5. slice is the one that has the maximum lookup events

Mapping physical addresses to slices



The gory details (1)

Accessing the performance counters

- program *Model Specific Registers* (MSRs) manually
- documentation in Intel Manual vol 3 (only 1914 pages!)
- code provided at `https://github.com/clementine-m/msr-uncore-cbo`

The gory details (2)

`monitoring.c`

1.	disable counters	write to `MSR_UNC_PERF_GLOBAL_CTRL`
2.	reset counters	write to `MSR_UNC_CBO_i_PER_CTR0` for each CBo i
3.	select event to monitor	write to `MSR_UNC_CBO_i_PERFEVTSEL0` for each CBo i
4.	enable counting	write to `MSR_UNC_PERF_GLOBAL_CTRL`
5.	function to monitor	cause access to address
6.	read counters	read `MSR_UNC_CBO_i_PER_CTR0` for each CBo i

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- create a *mapping table* for each *physical address* (with a 64B stride) to a *slice*

A few tips

Performance counters via MSRs monitor *every* event on your CPU $\rightarrow$ *noise*

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- verify your table matches known functions [Mau+15]
- functions from [Mau+15] are valid for Sandy Bridge, Ivy Bridge, Haswell and Broadwell

Method #2: Flush+Flush [Gru+16]

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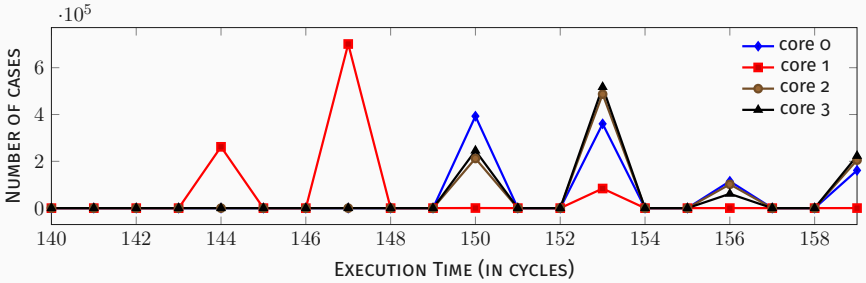
- time difference between *slices*

Last-level cache and Ring interconnect

Intel Optimization Manual:

“The LLC hit latency [...] depends on the core location relative to the LLC block, and *how far the request needs to travel on the ring*.”

clflush time difference between slices



clflush histogram for an address in slice 1 on different cores

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- timing attack: first phase is…?
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  - for each slice: local and remote slices
- find a threshold to distinguish a hit on *remote* slice vs *local* slice

Building the histogram

repeat:

1. measure time
2. flush a line (“flush hit”)
3. measure time
4. update histogram with delta
5. access the line twice

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3. decide which core corresponds to the local slice using threshold

$\rightarrow$ *local* slice = slice with *fastest* hits

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- similar to the method using `clflush`
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  - longer

Inferring the function

Two cases:

1. linear function: 2^n number of cores
2. non-linear function: the rest

Methods

- brute-force
- faster method

Perspective: both methods assume that we know what the functions look like (XORs of address bits)

Brute force

For each bit of output $o_0, \ldots, o_{k-1}$

1. try one function

$\rightarrow$ e.g., $b_6 \oplus b_7 \oplus \ldots \oplus b_{32}$

2. test if the function corresponds to the mapping you already have

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Fail fast, but still tolerate some errors

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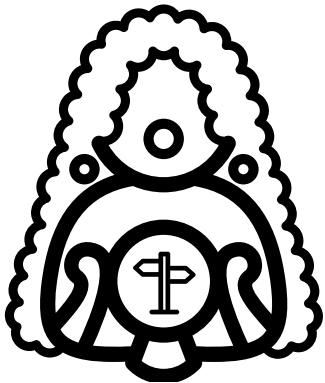
- XOR is associative: $A \oplus (B \oplus C) \Leftrightarrow (A \oplus B) \oplus C$
- you can treat all the input bits independently

Finding linear function (2/2) [Mau+15]

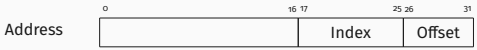
For each bit of output $o_0, \ldots, o_{k-1}$

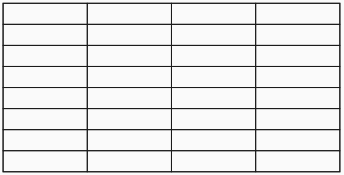
- find two addresses that differ by a single bit b_i
- compare output
  - if different: b_i is part of the function
  - if equal: b_i is not part of the function



Way Prediction

Set-Associative Caches





Cache

Set-Associative Caches

Data loaded in a specific set depending on its address

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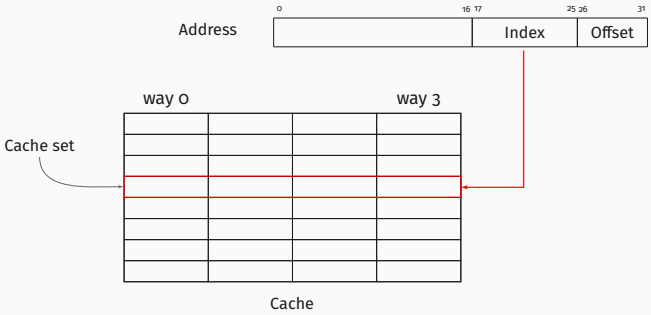

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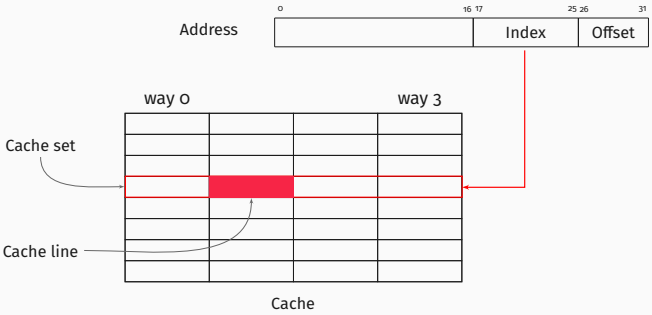

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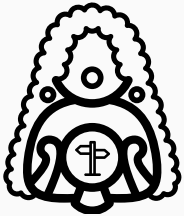

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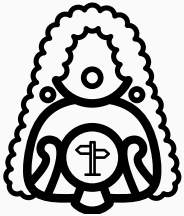

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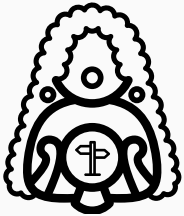

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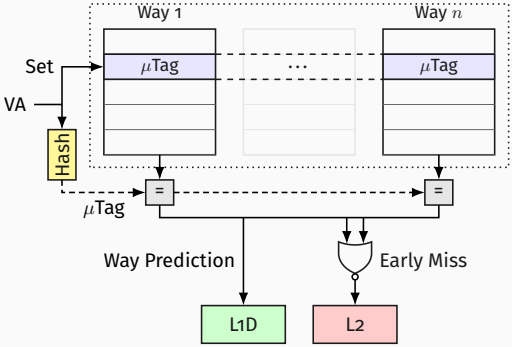
- Using **way prediction** [IIM99], one entry is predicted
  - Correct prediction: Access completed
  - Incorrect prediction: Perform associate check

AMD Way Predictor



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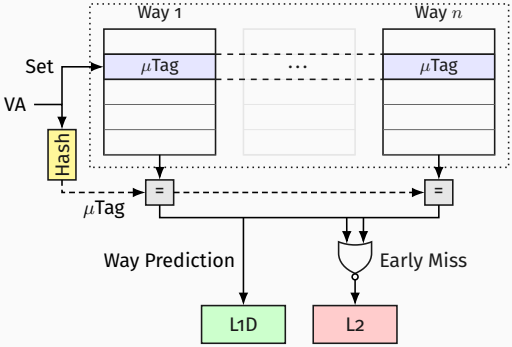

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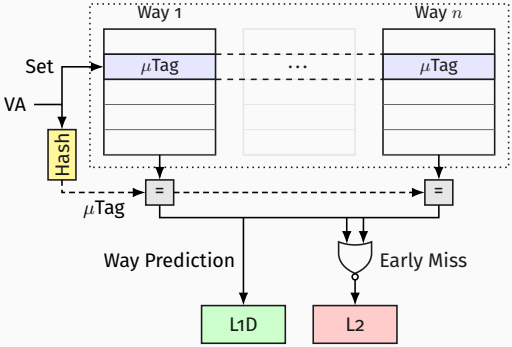

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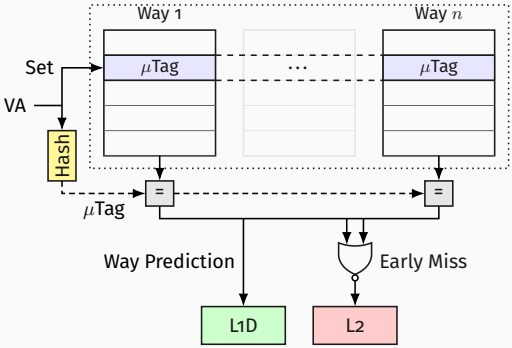

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- No match for μTag, detect early miss and issue L2 request

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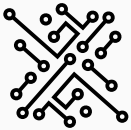

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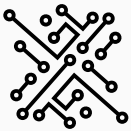

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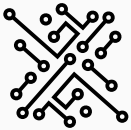
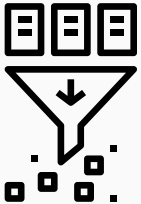


- Aliased cache lines can induce performance penalties
  - Two different virtual addresses that map to the same physical address
- Loads to an address that is valid in the L1D under a different alias will see an L1D miss
- Two different virtual addresses with the same μTag but different physical addresses will conflict

Hash Function



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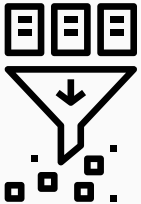

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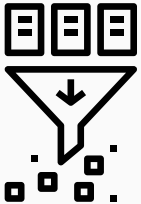

- L1D way predictor computes a hash (μTag) from the virtual address
- This hash function is **not documented**
  - Assume it is linear-based like other hash functions (cache slices, DRAM mapping, …)
  - Expect the size of the μTag to be a power of 2

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- If they have the **same μTag**:
  - Increased access time
  - Increased number of performance counter for L1 misses

Recovering the Hash Function

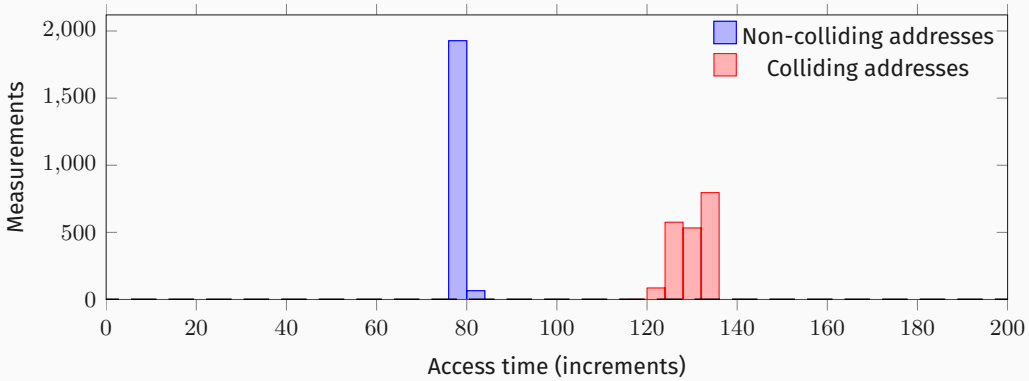
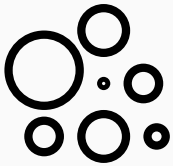


Figure 1: Measured duration of 250 alternating accesses to addresses with and without the same μTag.

Creating sets



Build n sets where n is the number of entries in the μTag table

1. Create pool v of virtual addresses which all map to the same cache set

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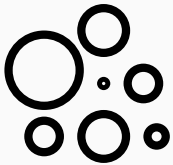

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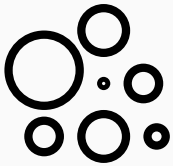

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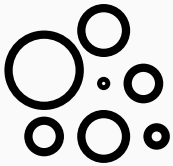

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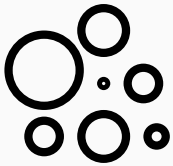
3. Repeat
   - Pick random address v_x
   - Measure access time of v_x and an address from each set $S_{0..n}$

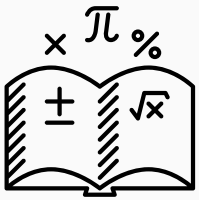
Creating sets



Build n sets where n is the number of entries in the μTag table

1. Create pool v of virtual addresses which all map to the same cache set
2. Start with one set S_0 containing one address from v
3. Repeat
   - Pick random address v_x
   - Measure access time of v_x and an address from each set $S_{0..n}$
   - If conflict, add to set. Otherwise, create new set containing v_x.

Recover hash function



- Every virtual address within a set produces the **same 8-bit hash**

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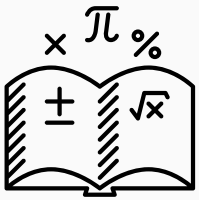

- Every virtual address within a set produces the **same 8-bit hash**
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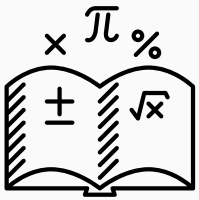
Recover hash function



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  - Over-determined linear equation system
  - b bits of virtual address a are coefficients, bits of the hash x are the unknown
  - For every address a in set s:

    $a_{b-1}x_{b-1} \oplus a_{b-2}x_{b-2} \oplus \cdots \oplus a_{12}x_{12} = y_s$

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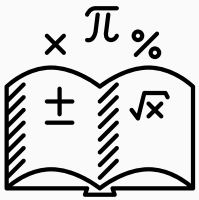

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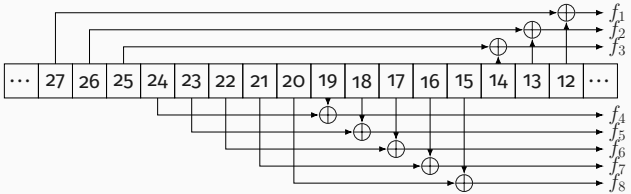
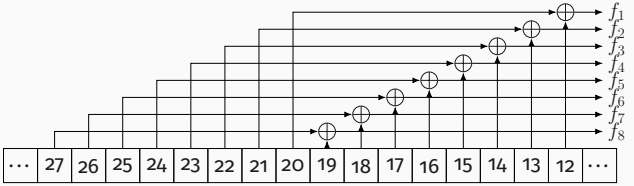
- Solve equation system using Z3 SAT solver

Recovering the Hash Function



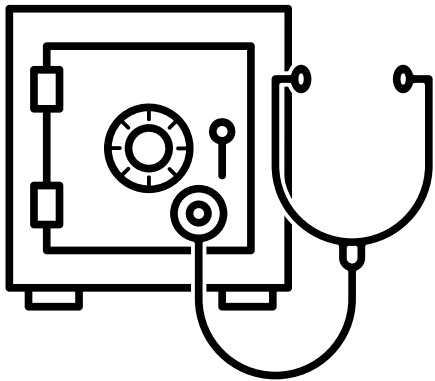
(a) Zen, Zen+, Zen 2



(b) Bulldozer, Piledriver, Steamroller

Microarchitectures

Setup	CPU	μ-arch.	WP
Lab	AMD Athlon 64 X2 3800+	K8	✗
Lab	AMD Turion II Neo N40L	K10	✗
Lab	AMD Phenom II X6 1055T	K10	✗
Lab	AMD E-450	Bobcat	✗
Lab	AMD Athlon 5350	Jaguar	✗
Lab	AMD FX-4100	Bulldozer	✓
Lab	AMD FX-8350	Piledriver	✓
Lab	AMD A10-7870K	Steamroller	✓
Lab	AMD Ryzen Threadripper 1920X	Zen	✓
Lab	AMD Ryzen Threadripper 1950X	Zen	✓
Lab	AMD Ryzen Threadripper 1700X	Zen	✓
Lab	AMD Ryzen Threadripper 2970WX	Zen+	✓
Lab	AMD Ryzen 7 3700X	Zen 2	✓
Cloud	AMD EPYC 7401p	Zen	✓
Cloud	AMD EPYC 7571	Zen	✓



Way Predictor for Side Channels

Collide+Probe

- Exploit μTag collisions in L1D cache way predictor

Collide+Probe

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- Does not require physical address information like Prime+Probe or specific instructions like Flush+Reload

Collide+Probe

- Exploit μTag collisions in L1D cache way predictor
- Does not require physical address information like Prime+Probe or specific instructions like Flush+Reload
- Does not work cross core and requires a high resolution timer

Collide+Probe

Attacker selects v' with the same μTag as the target address

- **Phase 1: Collide**: Access v' to update the way predictor

Collide+Probe

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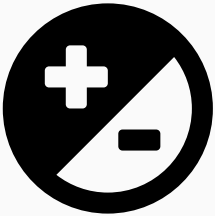
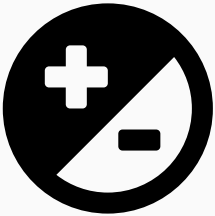
Collide+Probe: Pros and Cons



Pros:

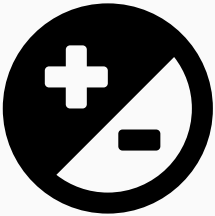
Collide+Probe: Pros and Cons



Pros:

- No knowledge of physical addresses required

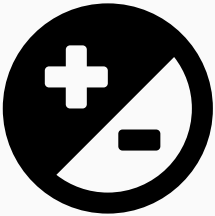
Collide+Probe: Pros and Cons



Pros:

- No knowledge of physical addresses required
- Single memory load is enough

Collide+Probe: Pros and Cons



Pros:

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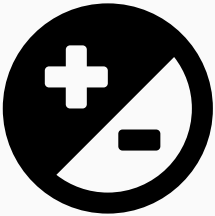

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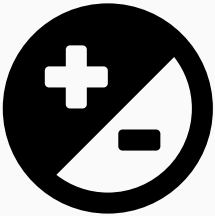

Pros:

- No knowledge of physical addresses required
- Single memory load is enough
- No clflush, no shared memory required

Cons:

- Timing difference between L1D and L2 hit is small

Load+Reload

- Exploit behavior for aliased addresses, *i.e.*, virtual addresses mapping to the same physical addresses

Load+Reload

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- Evict shared data used by the sibling thread with **single load**

Load+Reload

- **Phase 1: Load**: Load address v' with the same physical tag as v.

Load+Reload

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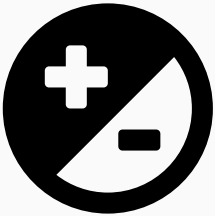

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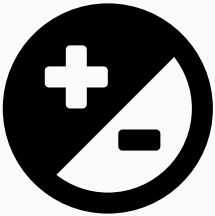

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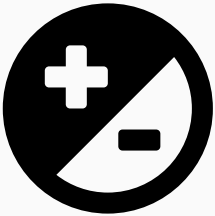
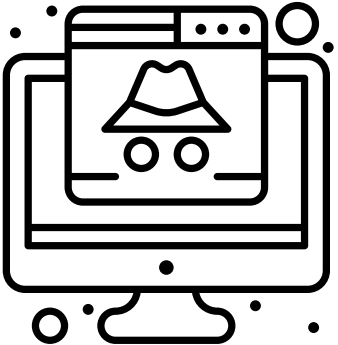


Pros:

- Only evicts from L1D

Cons:

- Only applicable in cross-thread scenario



Case Studies

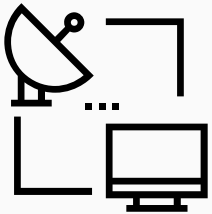
Covert Channel

- Communication Channel between two parties that are not allowed to communicate

Covert Channel

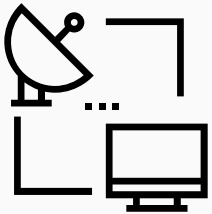
- Communication Channel between two parties that are not allowed to communicate
- Leveraging a side channel

Covert Channel



- 2 Processes accessing addresses with the same μTag and cache set
  - **Send a 1**: Access address
  - **Send a 0**: Don't access address

Covert Channel



- 2 Processes accessing addresses with the same μTag and cache set
  - **Send a 1**: Access address
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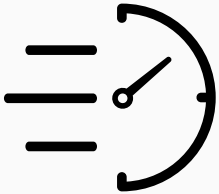
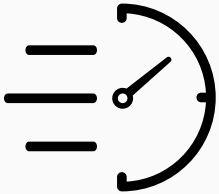
- Receiver measures timing difference and can deduce transmitted bit

Covert Channel



- Transmit multiple bits in parallel by utilizing multiple cache sets

Covert Channel



- Transmit multiple bits in parallel by utilizing multiple cache sets
- Maximum transmission rate of $588.9\,\mathrm{kB/s}$

Performance

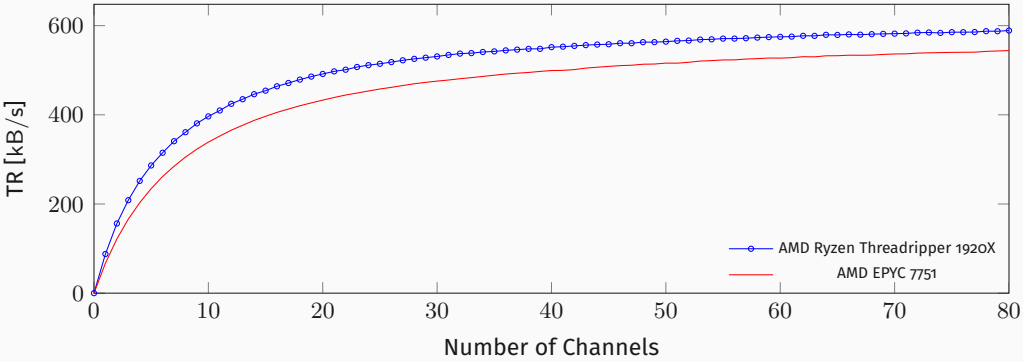


Figure 3: Mean transmission rate of the covert channels using multiple parallel channels on different CPUs.

Error Correction

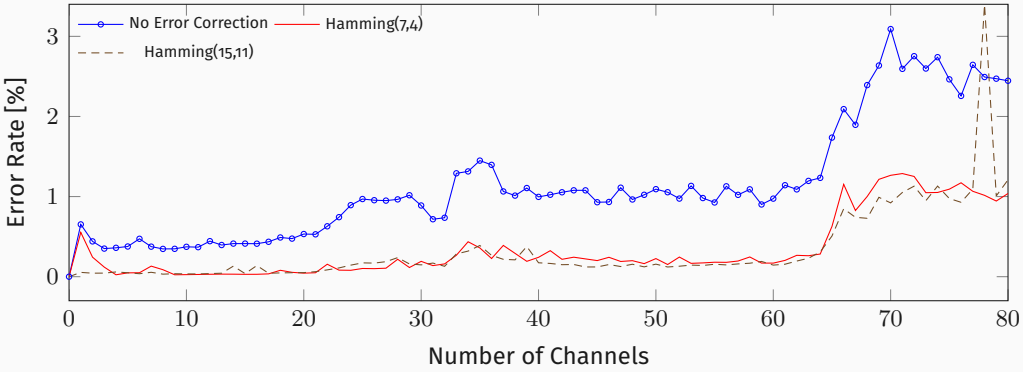
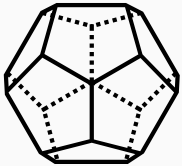


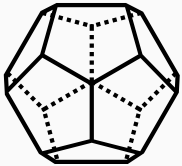
Figure 4: Error rate of the covert channel with and without error correction using different Hamming codes.

Breaking KASLR



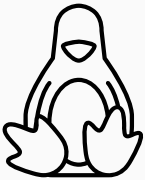
- Address Space Layout Randomization (ASLR) randomizes the location of memory sections to impede the exploitation of memory corruption vulnerabilities

Breaking KASLR



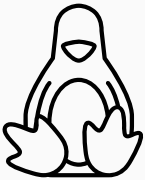
- Address Space Layout Randomization (ASLR) randomizes the location of memory sections to impede the exploitation of memory corruption vulnerabilities
- Exploit relation between μTags and virtual addresses to reduce entropy
  - Determine the μTag accessed by the victim
  - Use mapping function to infer bits of the address

Breaking KASLR



- Linux kernel is mapped using $2\,\mathrm{MB}$ pages
  - 512 different locations
  - 9 bits of entropy

Breaking KASLR



- Linux kernel is mapped using $2\,\mathrm{MB}$ pages
  - 512 different locations
  - 9 bits of entropy
- 21 lower bits of a **global variable** are identical to the offset within the kernel image

Breaking KASLR

- **Defeat KASLR**: Know offset of a global variable accessed by the kernel on a triggerable event

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- `SYS_time` system call returns the global second counter

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Breaking KASLR

$$v_{20} = v_{15} \oplus t_3 \qquad v_{21} = v_{16} \oplus t_4 \qquad v_{22} = v_{17} \oplus t_5$$
$$v_{23} = v_{18} \oplus t_6 \qquad v_{24} = v_{19} \oplus t_7 \qquad v_{25} = v_{14} \oplus t_2$$
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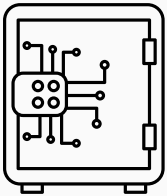
- Compute **bits 21 to 27** using the reverse-engineered hash function
- Reduce to 4 different locations (as bits 28 and 29 remain unknown)
- Average runtime of 0.51 ms and success rate of $98.5\,\%$

Other scenarios

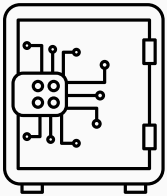
- **Hypervisor**: Leak base address of the KVM kernel module from a guest virtual machine
- **JavaScript**: Recover address bits of start of a typed array
- **User space**: Break heap ASLR using a high-speed API interface

Attacking AES T-Tables

- AES T-Tables: Fast software implementation



Attacking AES T-Tables



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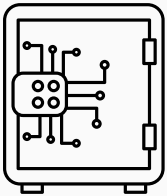

- AES T-Tables: Fast software implementation
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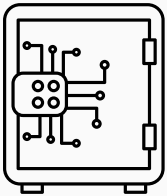
- One-round known-plaintext attack by Osvik et al. (2006) [OST06]
  - p plaintext and k secret key
  - Intermediate state $x^{(r)} = (x_0^{(r)}, \ldots, x_{15}^{(r)})$ at each round r
  - First round, accessed table indices are

$$x_i^{(0)} = p_i \oplus k_i \qquad \text{for all } i = 0, \ldots, 15$$

Attacking AES T-Tables



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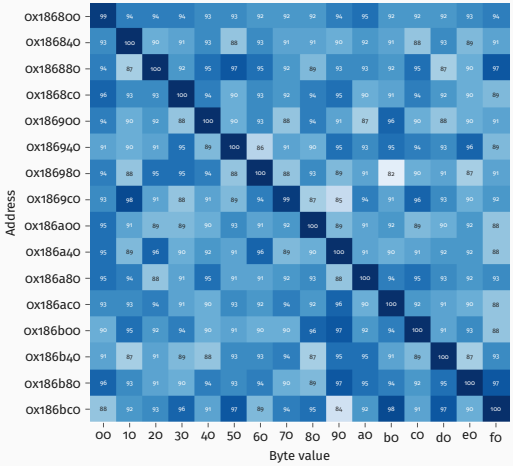
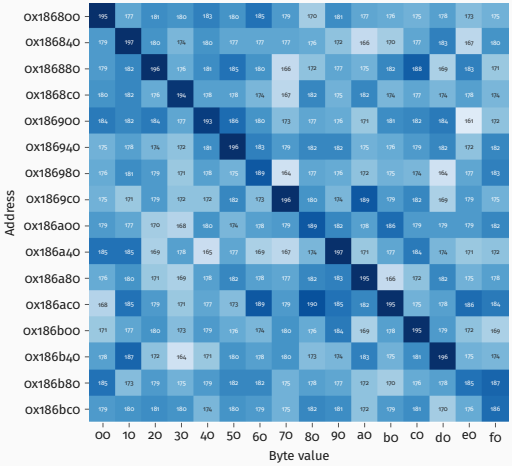
$\rightarrow$ Recovering accessed table indices $\Rightarrow$ recovering the key

Attacking AES T-Tables

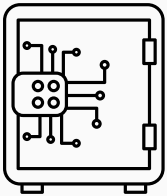


(a) Collide+Probe



(b) Load+Reload

Attacking AES T-Tables



- **Collide+Probe**: $168\,867$ encryptions per byte in $0.07\,\mathrm{s}$
- **Load+Reload**: $367\,731$ encryptions per byte in $0.53\,\mathrm{s}$
- **L1-Prime+Probe**: $450\,406$ encryptions per byte in $1.23\,\mathrm{s}$

Side-Channel Security

Chapter 3: Reverse Engineering Intel Last-Level Cache Mapping + AMD Way Predictor

Claudio Canella

March 16, 2021

Graz University of Technology

References i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