# Side-Channel Security

## Chapter 2: Cache Template Attacks

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# TLB and Paging

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- TLB (translation lookaside buffer) caches virtual to physical mapping
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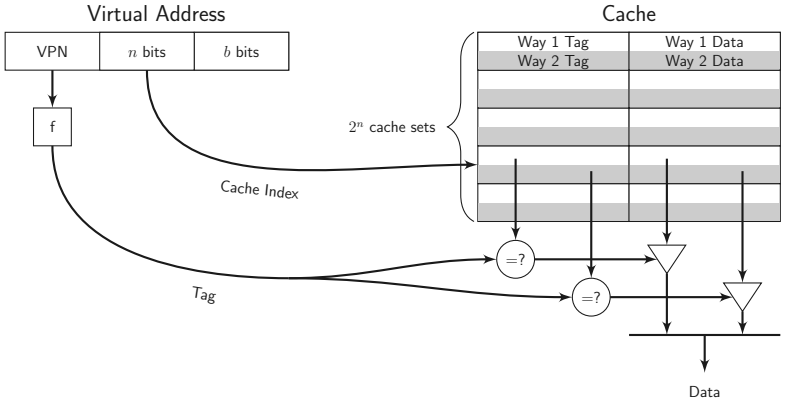
- TLB (translation lookaside buffer) caches virtual to physical mapping
- TLB has some latency
- Worst case for Cache: mapping not in TLB, need to load mapping from RAM
- Solution: Use virtual addresses instead of physical addresses

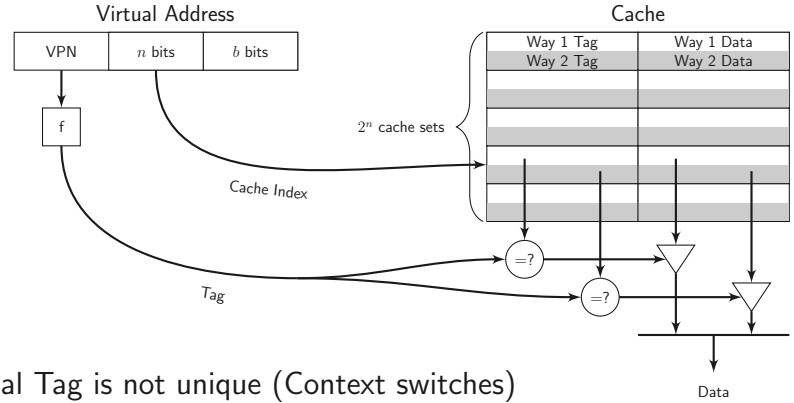
# Cache indexing methods

- VIVT: Virtually indexed, virtually tagged
- PIPT: Physically indexed, physically tagged
- PIVT: Physically indexed, virtually tagged
- VIPT: Virtually indexed, physically tagged

# VIVT

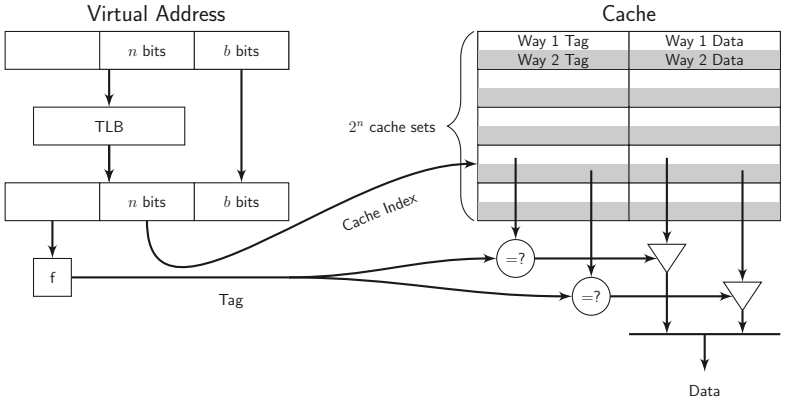

Virtual Address
VPN
n bits
b bits
f
Cache
Way 1 Tag
Way 2 Tag
Way 1 Data
Way 2 Data
2^n cache sets
Cache Index
Tag
=?
=?
Data

# VIVT




- Fast
- Virtual Tag is not unique (Context switches)
- Shared memory more than once in cache

# PIPT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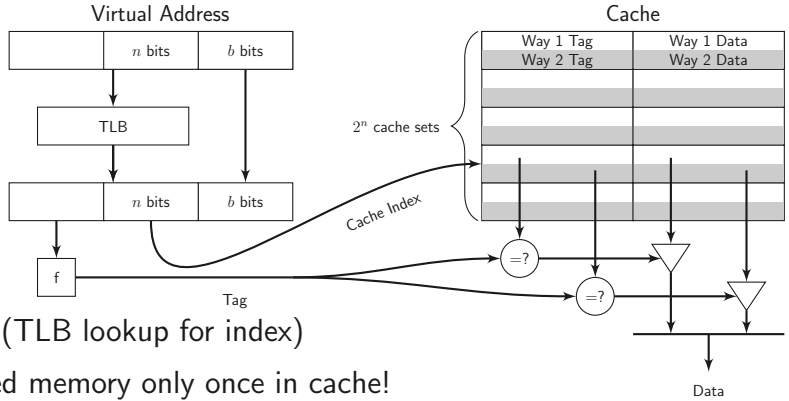
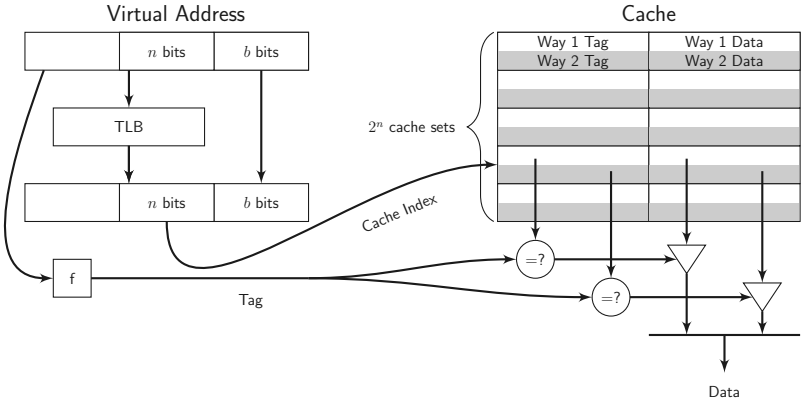



- Slow (TLB lookup for index)
- Shared memory only once in cache!

# (PIVT)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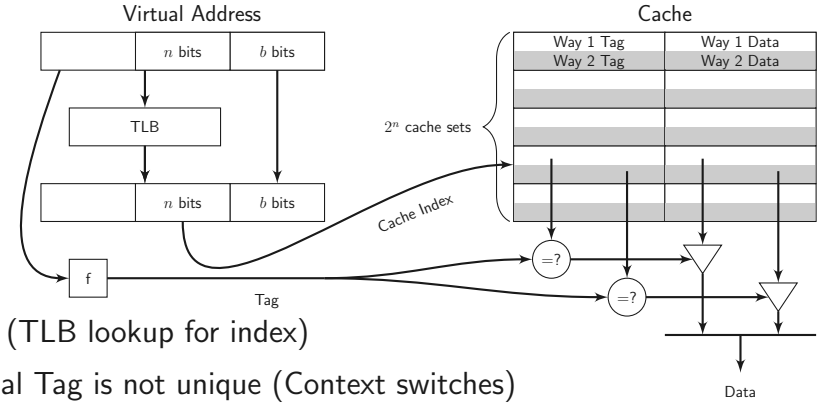


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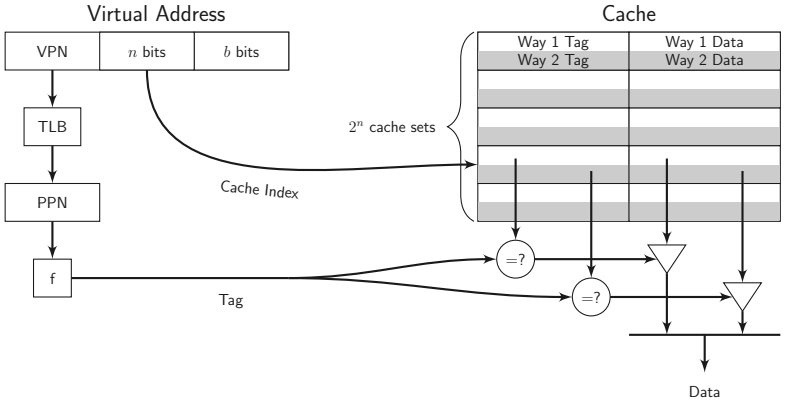
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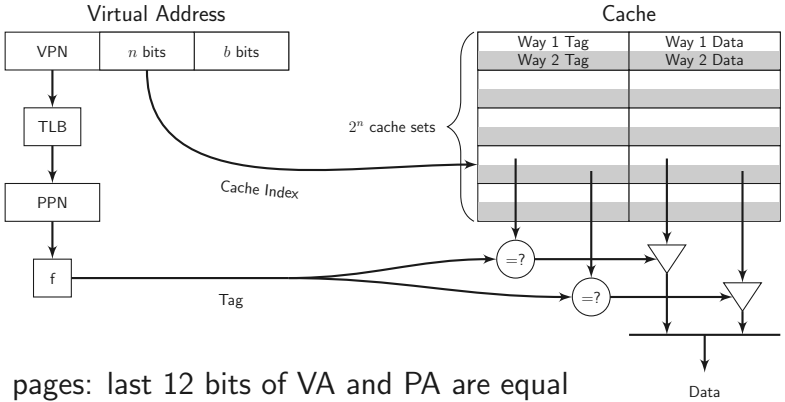


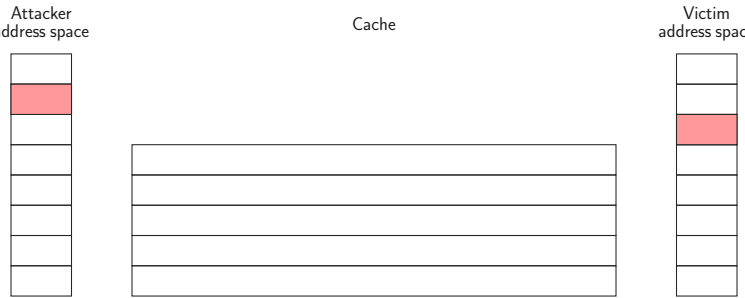

- Fast
- 4 KiB pages: last 12 bits of VA and PA are equal
- Using more bits is unpractical (like VIVT)

$\rightarrow$ Cache size $\leq$ # ways $\cdot$ page size

# Remarks

- L1 caches: VIVT or VIPT
- L2/L3 caches: PIPT

# Flush+Reload




**step 0**: attacker maps shared library → shared memory, shared in cache

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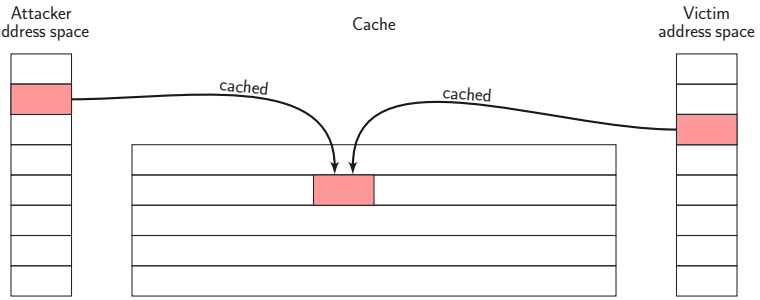


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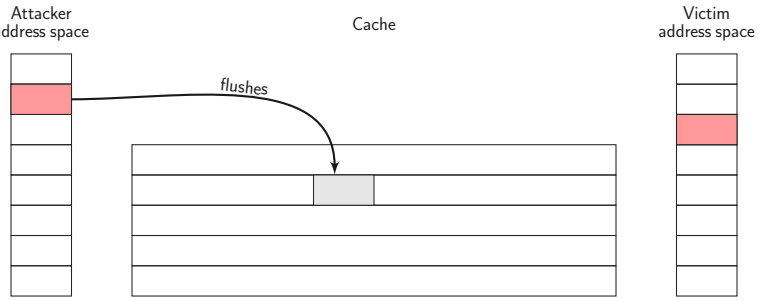


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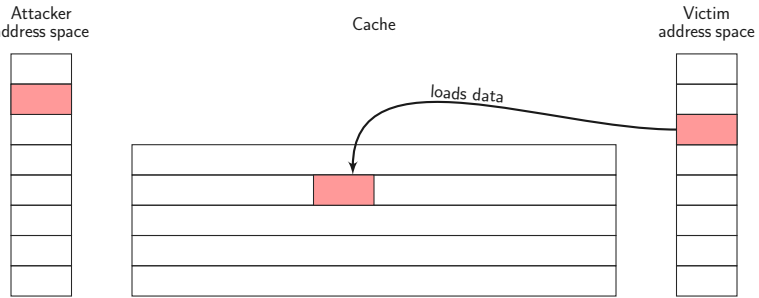


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**step 2**: victim loads data while performing encryption

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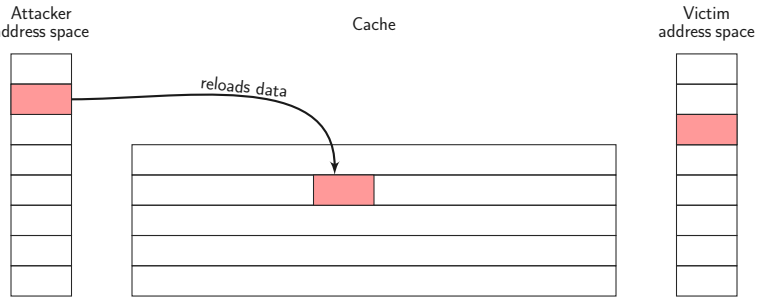



**step 0**: attacker maps shared library → shared memory, shared in cache

**step 1**: attacker flushes the shared line

**step 2**: victim loads data while performing encryption

**step 3**: attacker reloads data → fast access if the victim loaded the line

# Flush+Reload

Pros: fine granularity (1 line)

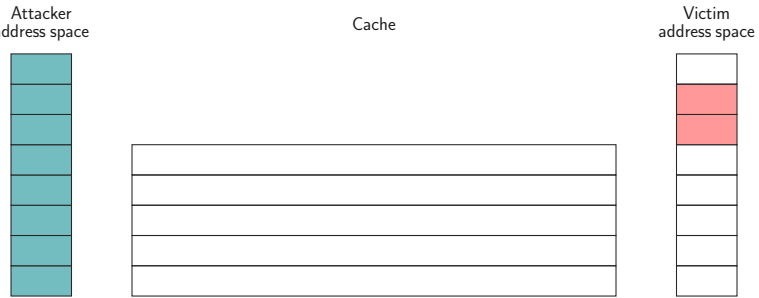
Cons: restrictive

1. needs `clflush` instruction (not available e.g., in JS)
2. needs shared memory

# Variants of Flush+Reload

- Flush+Flush [1]
- Evict+Reload [2] on ARM [4]

# Prime+Probe

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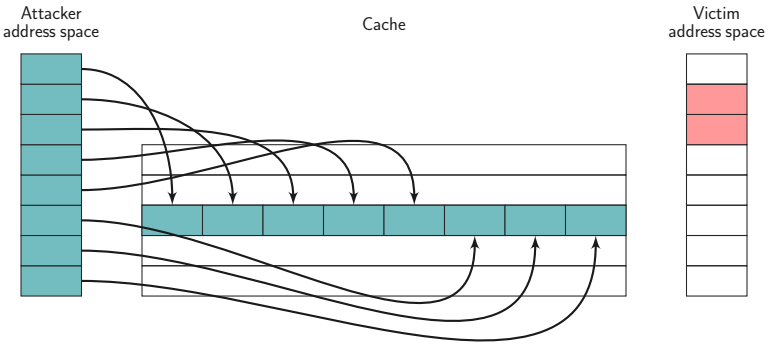


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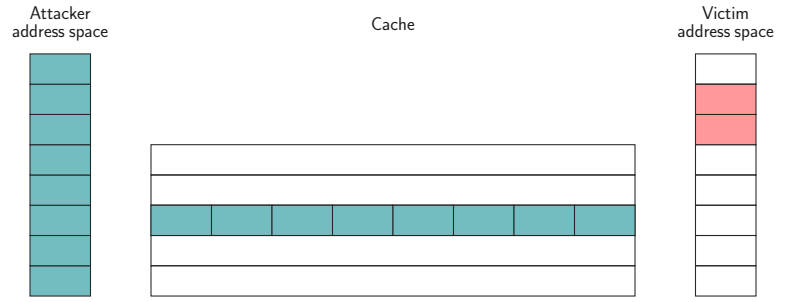


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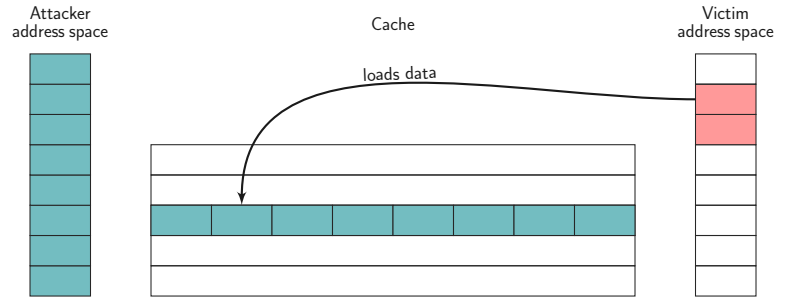


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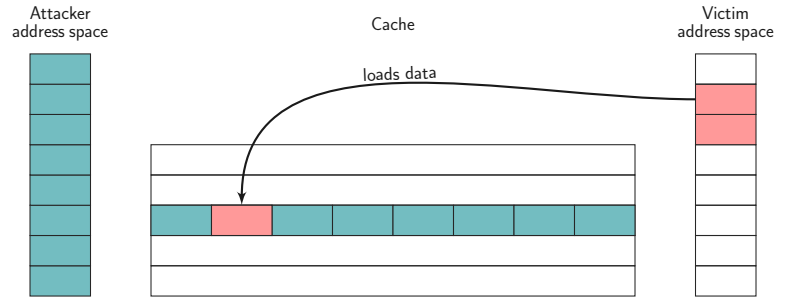


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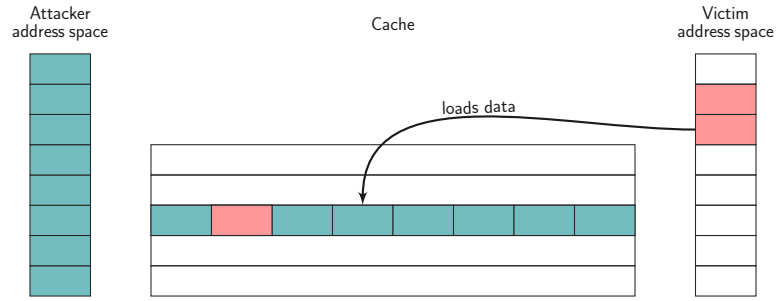


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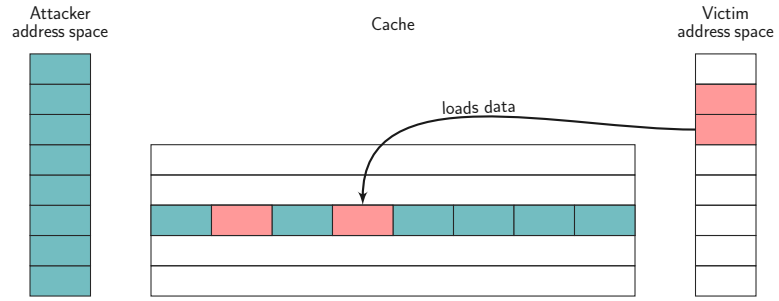


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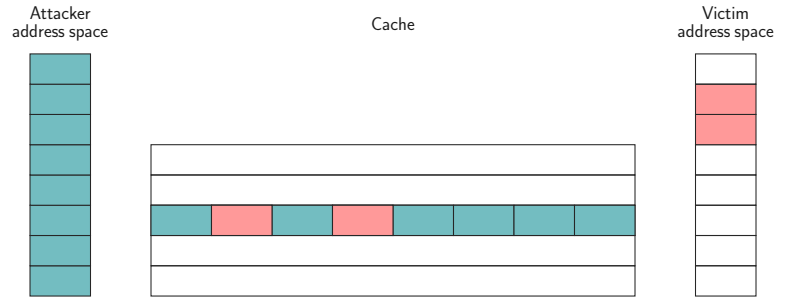


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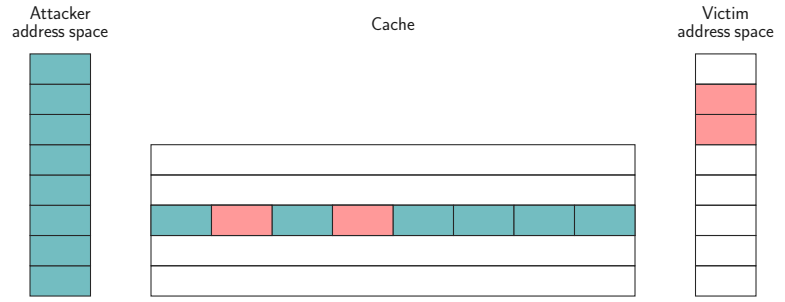


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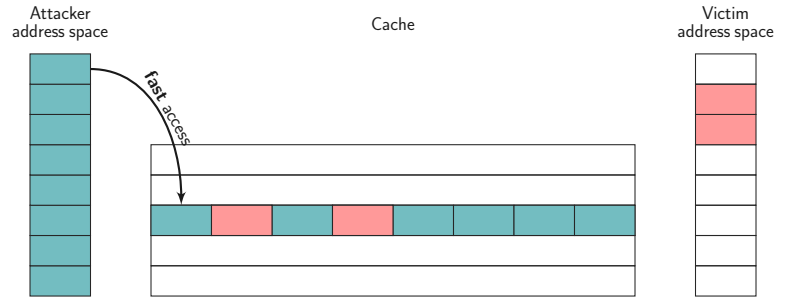


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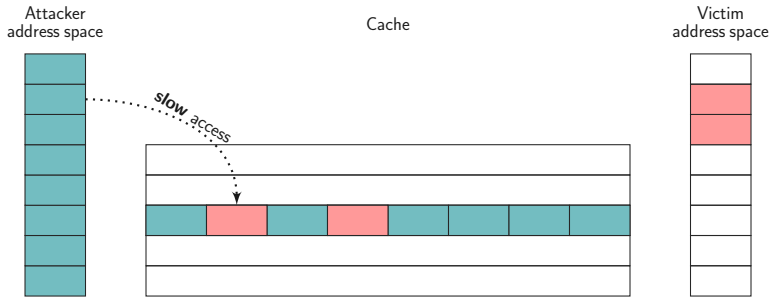


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# Prime+Probe

Pros: less restrictive

1. no need for `clflush` instruction (not available e.g., in JS)
2. no need for shared memory

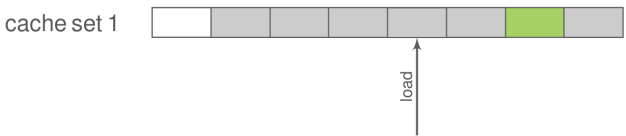
Cons: coarser granularity (1 set)

# Issues with Prime+Probe

We need to evict caches lines without `clflush` or shared memory:

1. which addresses do we access to have congruent cache lines?
2. without any privilege?
3. and in which order do we access them?

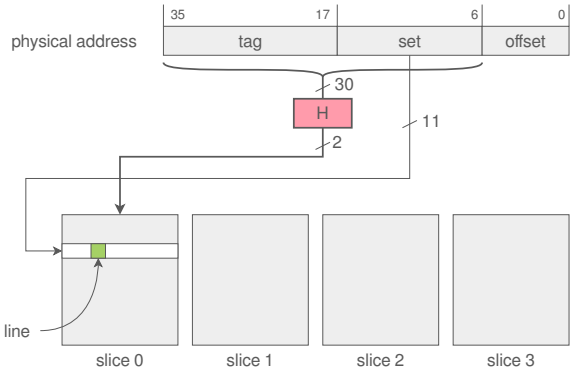
# #1.1: Which physical addresses to access?




"LRU eviction":

- assume that cache uses LRU replacement
- accessing $n$ addresses from the same cache set to evict an $n$-way set
- eviction from last level $\rightarrow$ from whole hierarchy (it's inclusive!)

# #1.2: Which addresses map to the same set?

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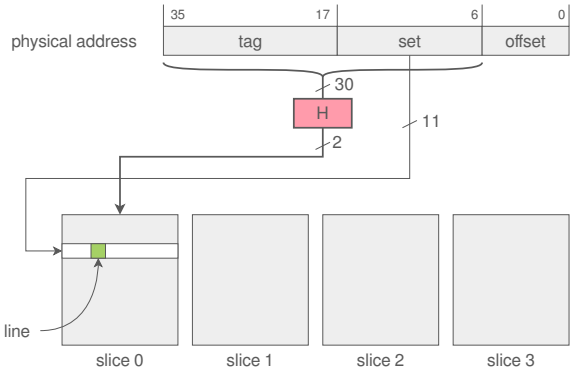


- function H that maps slices is undocumented
- reverse-engineered by [3, 6, 8]
- hash function basically an XOR of address bits

# #1.2: Which addresses map to the same set?

3 functions, depending on the number of cores

| | | Address bit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 |
| 2 cores | $o_0$ | | | | | | ⊕ | | ⊕ | | ⊕ | ⊕ | ⊕ | ⊕ | ⊕ | | ⊕ | | ⊕ | | ⊕ | ⊕ | ⊕ | | ⊕ | | ⊕ | | ⊕ | | | | ⊕ |
| 4 cores | $o_0$ | | | | | ⊕ | ⊕ | | ⊕ | | ⊕ | ⊕ | ⊕ | ⊕ | ⊕ | | ⊕ | | ⊕ | | ⊕ | ⊕ | ⊕ | | ⊕ | | ⊕ | | ⊕ | | | | ⊕ |
| | $o_1$ | | | | ⊕ | ⊕ | | ⊕ | | ⊕ | ⊕ | | ⊕ | | ⊕ | ⊕ | ⊕ | ⊕ | ⊕ | ⊕ | | ⊕ | | ⊕ | | ⊕ | | ⊕ | | | | ⊕ | |
| 8 cores | $o_0$ | | ⊕ | ⊕ | | ⊕ | ⊕ | | ⊕ | | ⊕ | ⊕ | ⊕ | ⊕ | ⊕ | | ⊕ | | ⊕ | | ⊕ | ⊕ | ⊕ | | ⊕ | | ⊕ | | ⊕ | | | | ⊕ |
| | $o_1$ | ⊕ | | ⊕ | ⊕ | ⊕ | | ⊕ | | ⊕ | ⊕ | | ⊕ | | ⊕ | ⊕ | ⊕ | ⊕ | ⊕ | ⊕ | | ⊕ | | ⊕ | | ⊕ | | ⊕ | | | | ⊕ | |
| | $o_2$ | ⊕ | ⊕ | ⊕ | ⊕ | | | ⊕ | ⊕ | | | ⊕ | ⊕ | | | ⊕ | ⊕ | | | ⊕ | | | ⊕ | | | ⊕ | ⊕ | | | | ⊕ | | |

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$\rightarrow$ enough to compute the cache set

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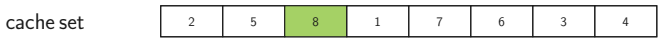


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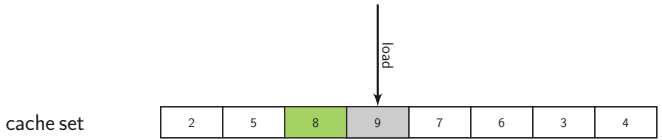


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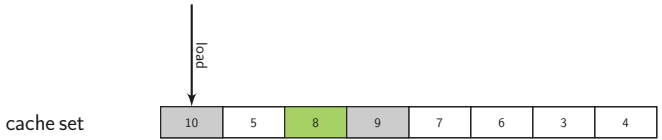


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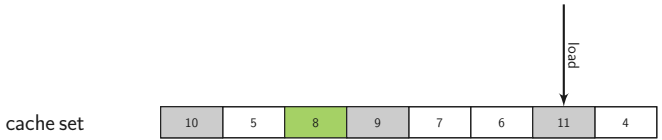


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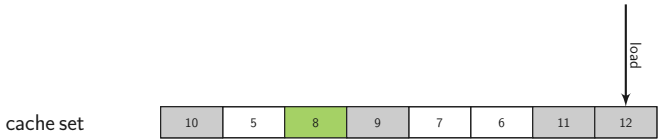


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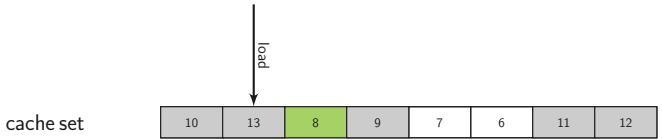


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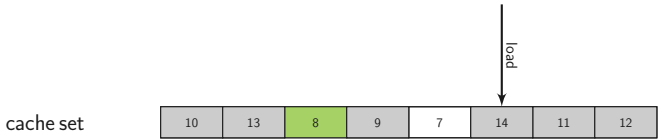


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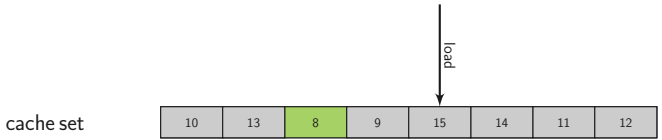


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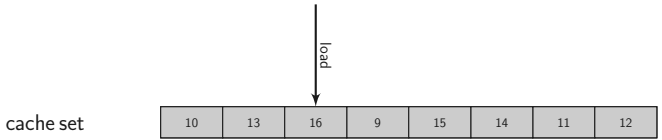


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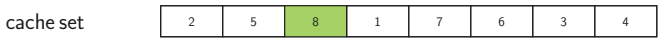


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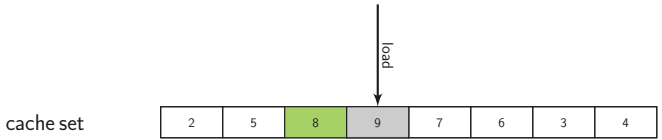


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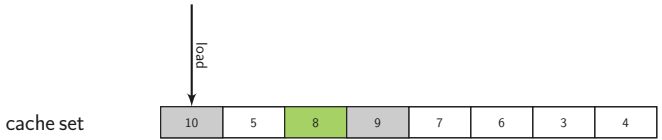


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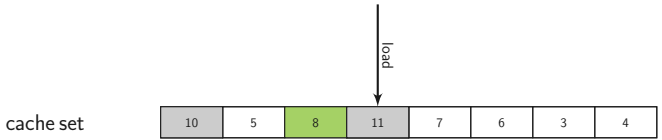


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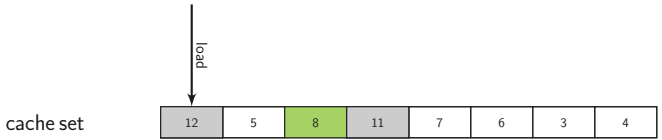


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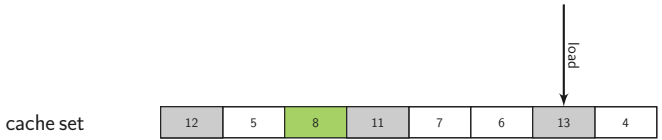


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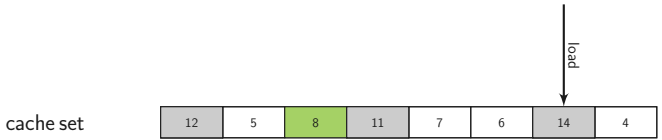


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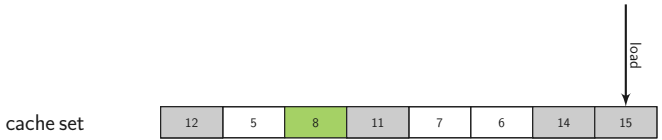


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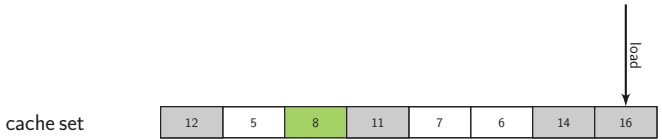


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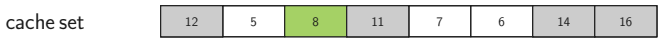


- no LRU replacement
- only 75% success rate on Haswell
- more accesses → higher success rate, but too slow

# #3.3: Cache eviction strategy

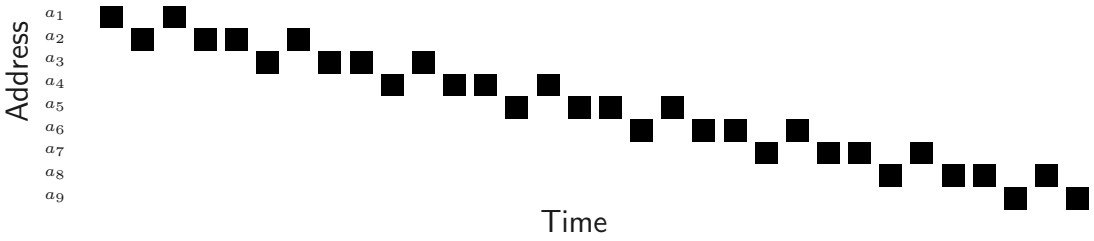


**Figure 1:** Fast and effective on Haswell. Eviction rate >99.97%.

# Cache covert channels

# Side channels vs covert channels

- side channel: attacker spies a victim process
- covert channel: communication between two processes
  - that are not supposed to communicate
  - that are collaborating

# 1-bit cache covert channels

ideas for 1-bit channels:

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- Prime+Probe: use one cache set to transmit
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ideas for 1-bit channels:

- Prime+Probe: use one cache set to transmit
  - 0: sender does not access the set → low access time in receiver
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- Flush+Reload/Flush+Flush/Evict+Reload: use one address to transmit
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# 1-bit covert channels

- 1 bit data, 0 bit control?

# 1-bit covert channels

- 1 bit data, 0 bit control?
- idea: divide time into slices (e.g., $50\mu s$ frames)
- synchronize sender and receiver with a shared clock

# Problems of 1-bit covert channels

- errors?

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- errors? $\rightarrow$ error-correcting codes
- retransmission may be more efficient (less overhead)
- desynchronization
- optimal transmission duration may vary

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- use 1-bit for sending = true/false

# Packets / frames

Organize data in packets / frames:

- some data bits
- check sum
- sequence number

$\rightarrow$ keep sender and receiver synchronous

$\rightarrow$ check whether retransmission is necessary

# Efficient retransmission

How can the sender know when to retransmit?

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- why wait for retransmission?

$\rightarrow$ sender should retransmit until receiver acknowledged

# Raw capacity $C$

- number of bits per second
- measure over $\geq 1$ minute

$s$ bits transmitted in 1 minute:

$$C = \frac{s}{60}$$

# Bit error rate $p$

- count bits that are wrong $w$
- count total bits sent $b_s$
- count total bits received $b_r$

Error rate:

$$p = \frac{w + |b_r - b_s|}{\max(b_s, b_r)},$$

or if $b_r = b_s$:

$$p = \frac{w}{b_r},$$

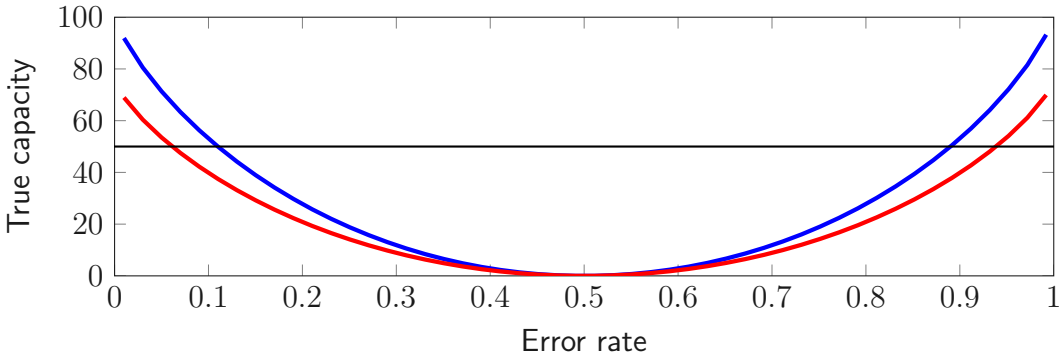
# Capacity

True capacity $T$:

$$T = C \cdot (1 + ((1 - p) \cdot \log_2 (1 - p) + p \cdot \log_2 (p)))$$

$C$ is the *raw capacity* and $p$ is the *bit error rate*.

# Capacity


True capacity
100
80
60
40
20
0
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Error rate

# State of the art

| method | raw capacity | err. rate | true capacity | env. |
|---|---|---|---|---|
| F+F [1] | 3968Kbps | 0.840% | 3690Kbps | native |
| F+R [1] | 2384Kbps | 0.005% | 2382Kbps | native |
| E+R [4] | 1141Kbps | 1.100% | 1041Kbps | native |
| P+P [7] | 601Kbps | 0.000% | 601Kbps | native |
| P+P [5] | 600Kbps | 1.000% | 552Kbps | virt |
| P+P [7] | 362Kbps | 0.000% | 362Kbps | native |

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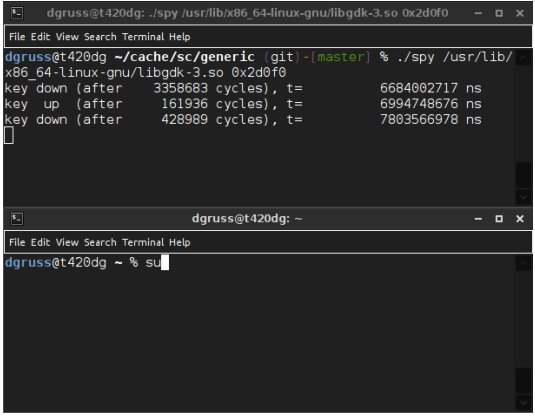
- Examples:
  - Cache-based keylogger
  - Automatic attacks on crypto algorithms

# Can We Build a Cache-Based Keylogger?



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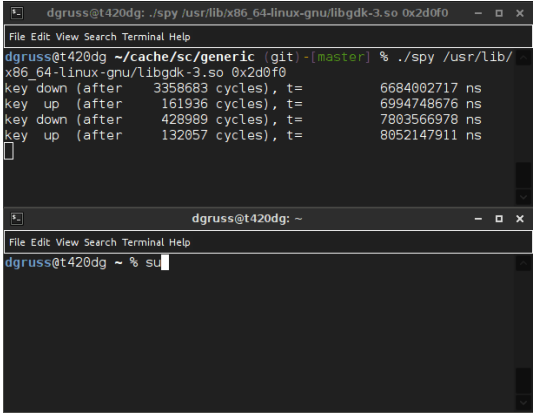

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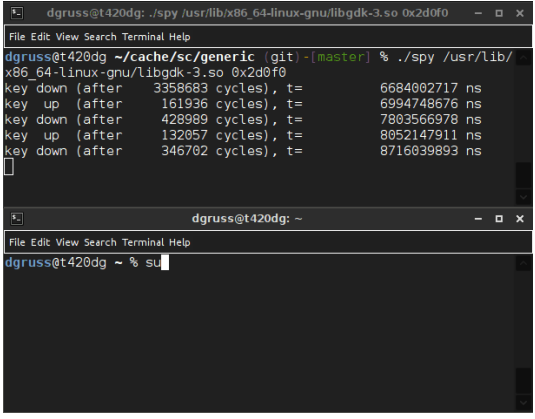

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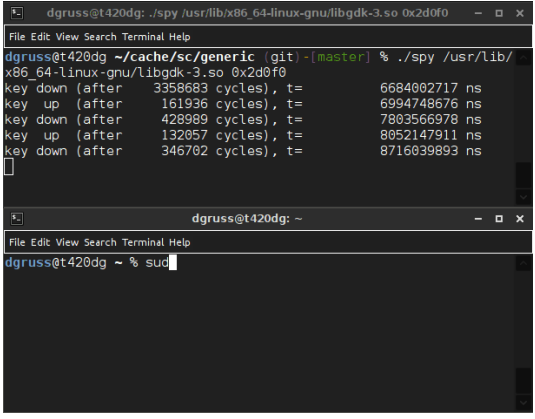

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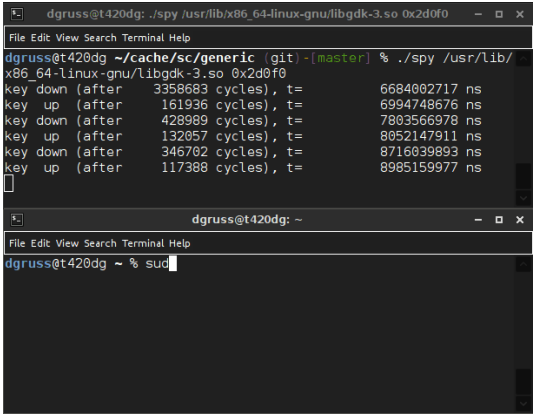

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- Difficult to find all exploitable addresses

# Cache Template Attacks

Profiling Phase

- Preprocessing step to find exploitable addresses automatically
  - w.r.t. “events” (keystrokes, encryptions, ...)
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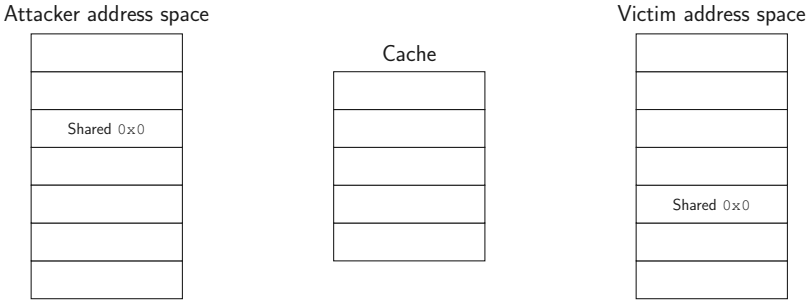
Exploitation Phase

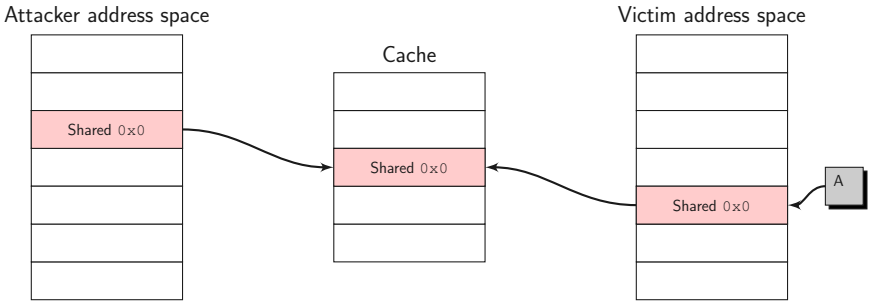
- Monitor exploitable addresses

# Profiling Phase



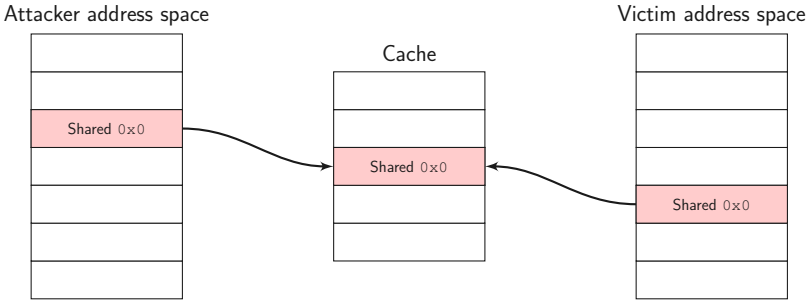

Cache is empty

# Profiling Phase



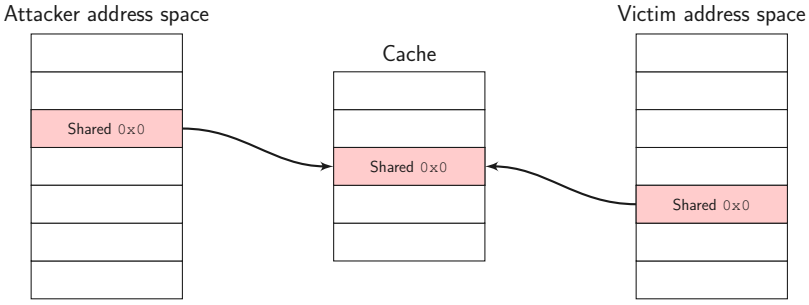

Attacker triggers an event

# Profiling Phase



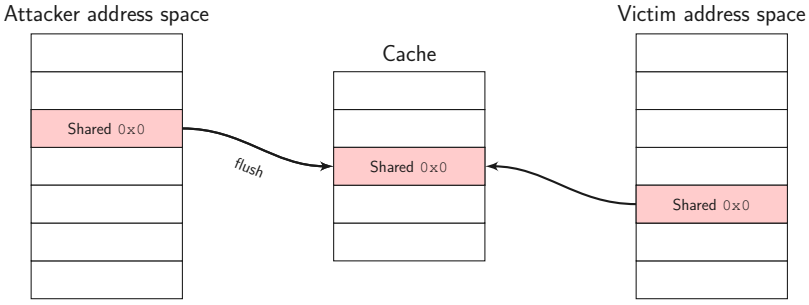

Attacker checks one address for cache hits ("Reload")

# Profiling Phase



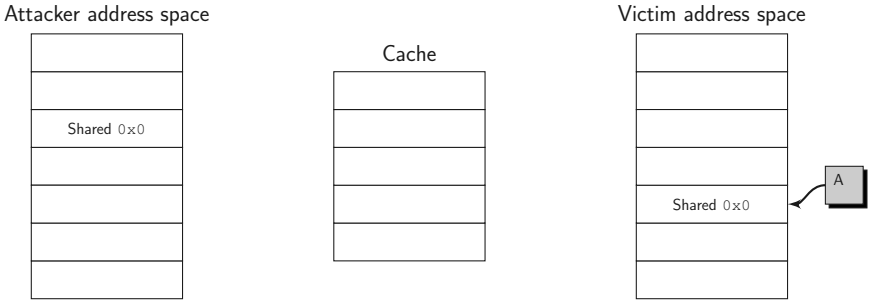

Update cache hit ratio (per event and address)

# Profiling Phase



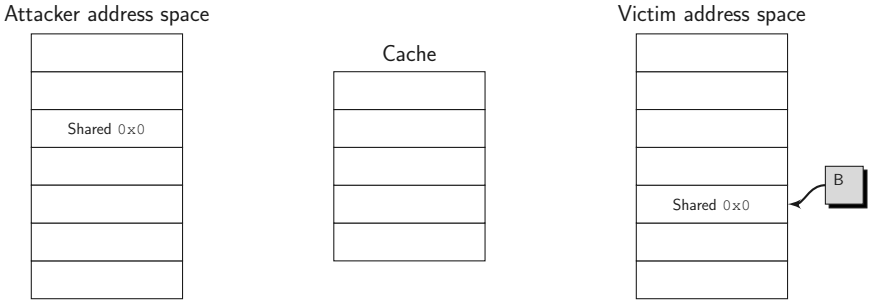

Attacker flushes shared memory

# Profiling Phase




Repeat for higher accuracy

# Profiling Phase




Repeat for all events

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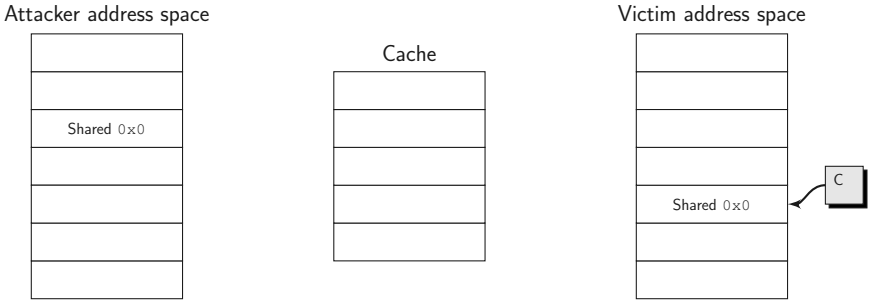


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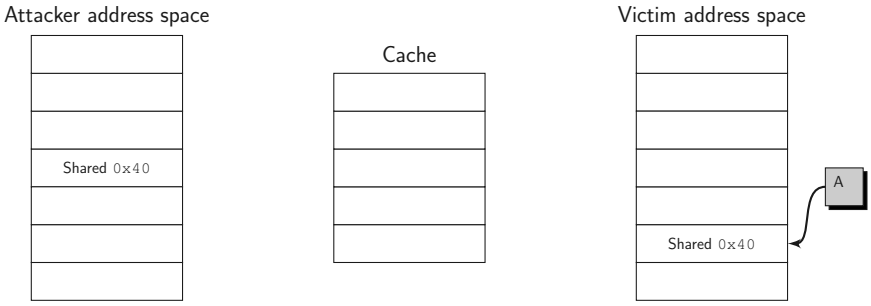


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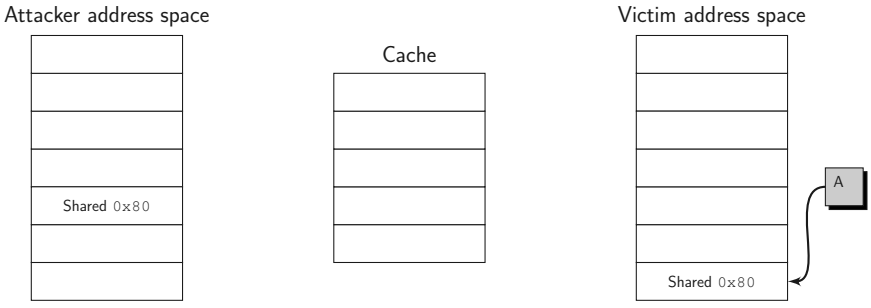


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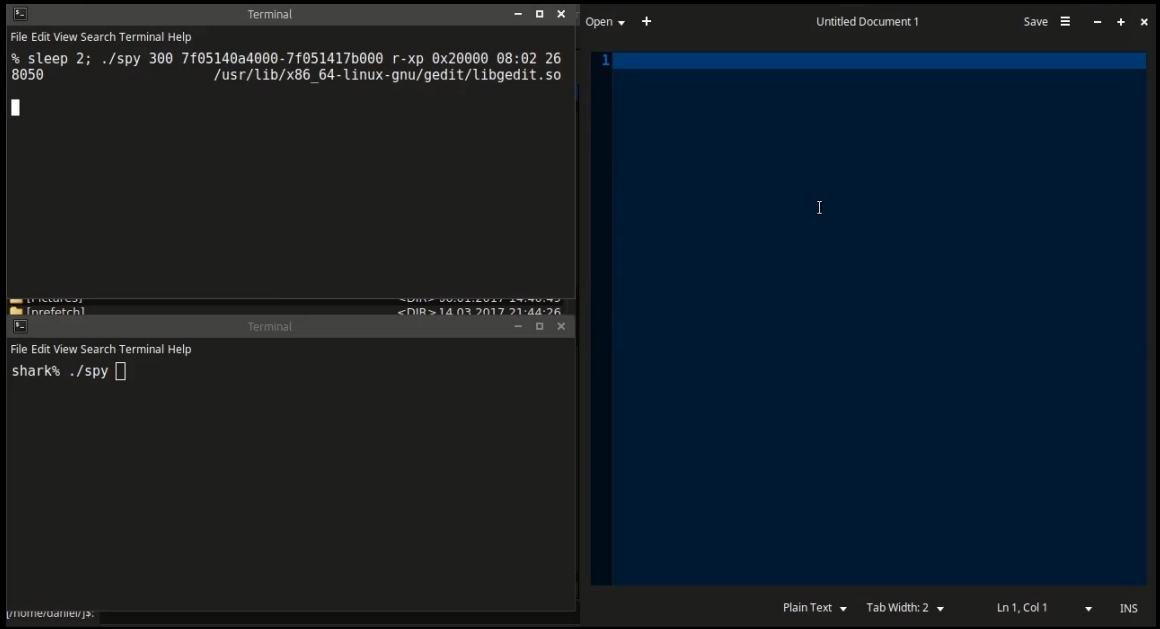
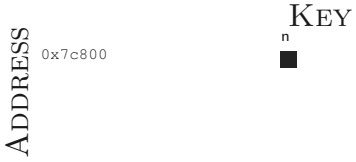



Cache Template Attack Demo

# Profiling Phase: 1 Event, 1 Address



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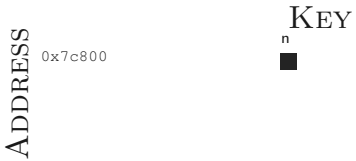


Example: Cache Hit Ratio for $(\texttt{0x7c800}, \texttt{n})$: 200 / 200

# Profiling Phase: All Events, 1 Address

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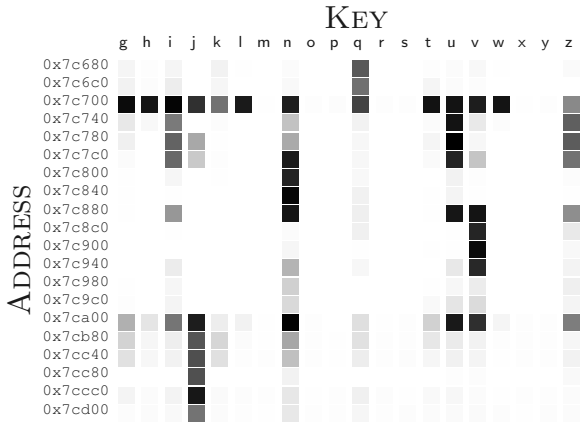
Example: Cache Hit Ratio for $(\texttt{0x7c800}, \texttt{u})$: 13 / 200

# Profiling Phase: All Events, 1 Address


Distinguish `n` from other keys by monitoring `0x7c800`

# Profiling Phase: All Events, All Addresses



# Attack 3: Locate AES T-Tables

AES uses T-Tables (precomputed from S-Boxes)

- 4 T-Tables
- $$T_0\left[k_{\{0,4,8,12\}} \oplus p_{\{0,4,8,12\}}\right]$$
  $$T_1\left[k_{\{1,5,9,13\}} \oplus p_{\{1,5,9,13\}}\right]$$
  ...
- If we know which entry of $T$ is accessed, we know the result of $k_i \oplus p_i$.
- Known-plaintext attack ($p_i$ is known) $\rightarrow$ $k_i$ can be determined

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- Most addresses in two groups:
  - Cache hit ratio $100\%$ (always cache hits)
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- One 4096 byte memory block:
  - Cache hit ratio of $92\%$
  - Cache hits depend on key value and plaintext value
  - The T-Tables

# Attack 4: AES T-Table Template Attack

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- Known-plaintext attack
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  - State of the art: full key recovery after 30000 encryptions

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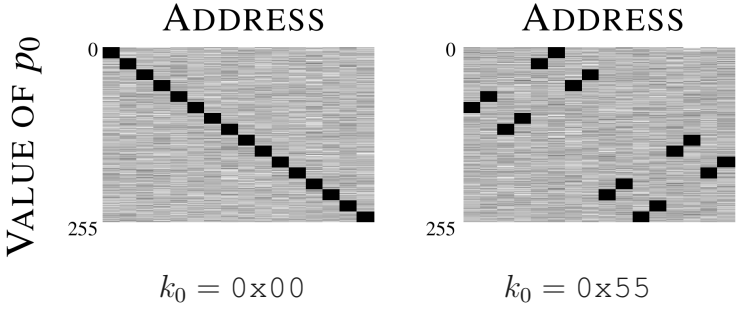


(transposed)

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- Marks a change of perspective:
  - Large scale analysis of binaries
  - Large scale automated attacks

# Evict+Reload

- Variant of Flush+Reload with cache eviction instead of `clflush`
- Works on ARMv7
- Applicable to millions of devices
- Cache Template Attacks using Evict+Reload
- ARMageddon: Last-Level Cache Attacks on Mobile Devices [4]

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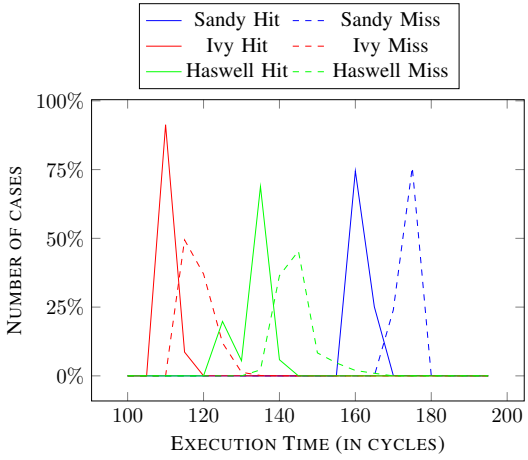
- causing a cache flush $\neq$ causing a cache miss

# `clflush` execution time



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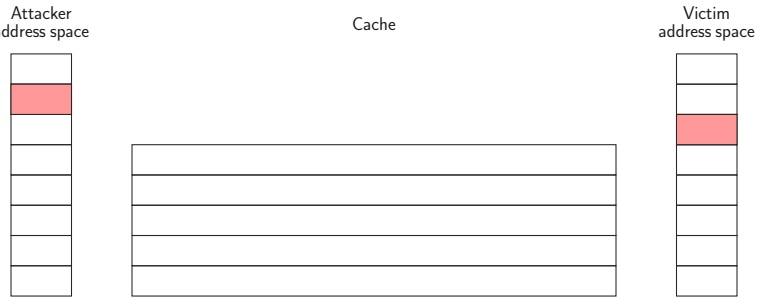

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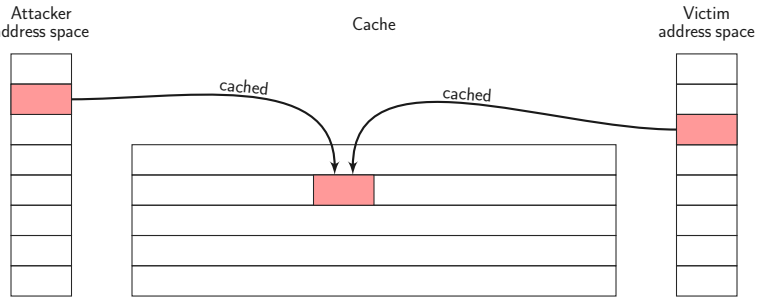
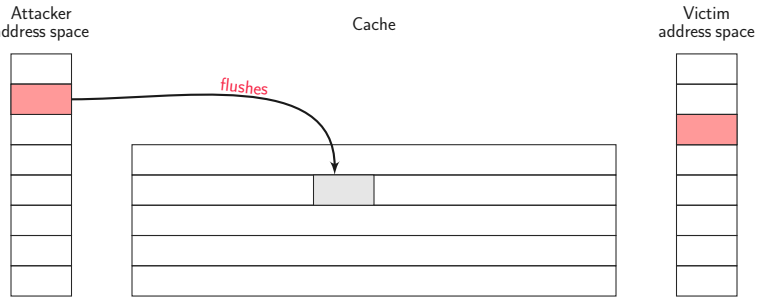
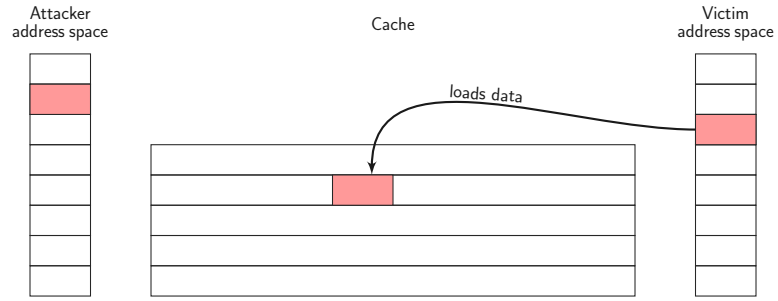

Attacker
address space
Cache
Victim
address space
cached
cached

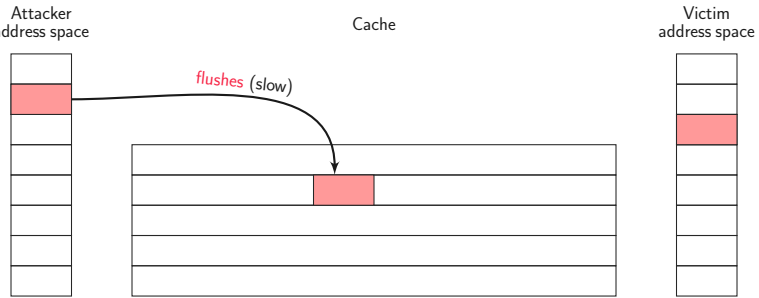
# Flush+Flush


Attacker
address space
Cache
Victim
address space
flushes

# Flush+Flush


Attacker
address space
Cache
Victim
address space
loads data

# Flush+Flush


Attacker
address space
Cache
Victim
address space
flushes (slow)

# Flush+Flush: Conclusion

- attacker causes no direct cache misses
  - $\rightarrow$ fast
  - $\rightarrow$ stealthy

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- 496 KB/s covert channel

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- powerful cache attacks on Intel x86 in the last 10 years
- nothing like Flush+Reload or Prime+Probe on mobile devices

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$\rightarrow$ why?

# ARMageddon in a nutshell

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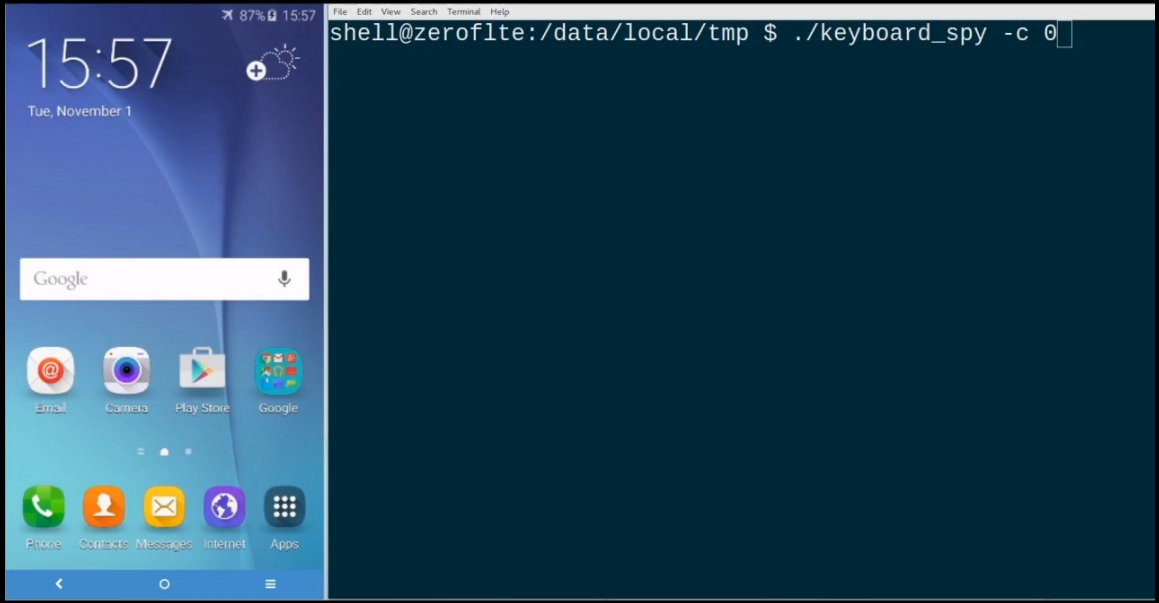


ARMageddon Demo

# Prefetch Side-Channel Attacks

# Overview

- prefetch instructions don't check privileges
- prefetch instructions leak timing information

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- prefetch instructions leak timing information

exploit this to:

- locate a driver in kernel = defeat KASLR
- translate virtual to physical addresses

# Intel being overspecific

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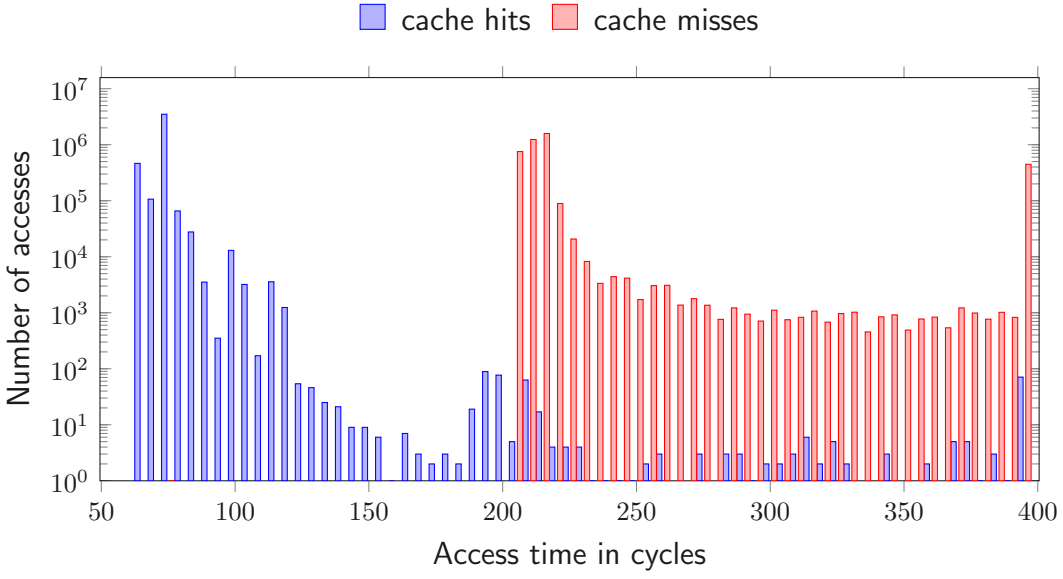
# CPU Caches

Memory (DRAM) is slow compared to the CPU

- buffer frequently used memory
- every memory reference goes through the cache
- based on physical addresses

# Memory Access Latency



# Unprivileged cache maintainance

Optimize cache usage:

- `prefetch`: suggest CPU to load data into cache
- `clflush`: throw out data from all caches

... based on virtual addresses

# Software prefetching

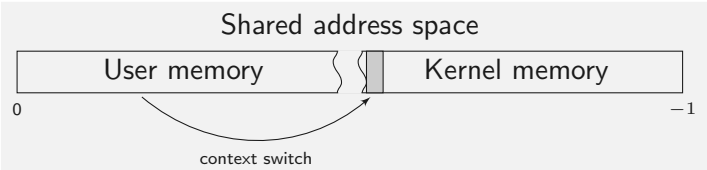
`prefetch` instructions are somewhat unusual

- hints – can be ignored by the CPU
- do not check privileges or cause exceptions

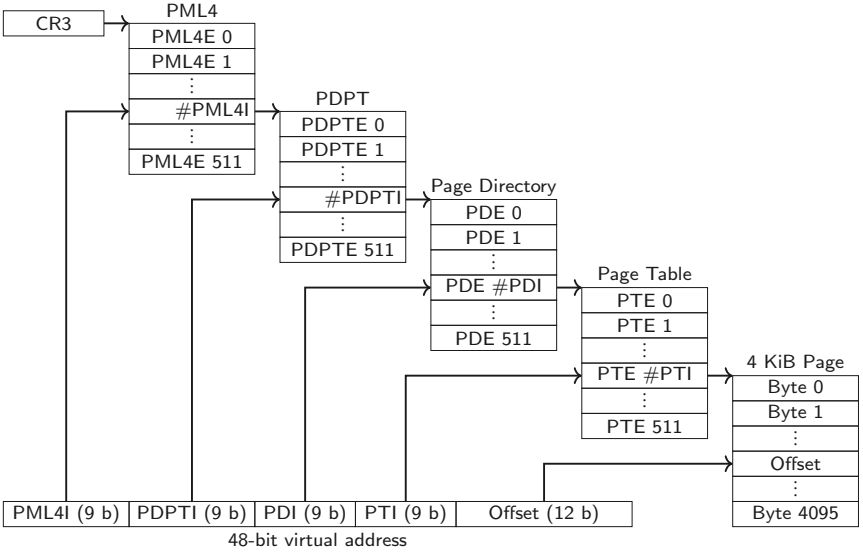
but they do need to translate virtual to physical

# Kernel must be mapped in every address space

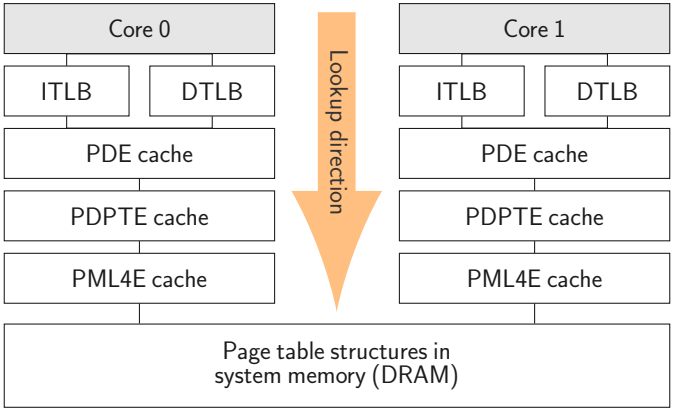
**Today's operating systems:**



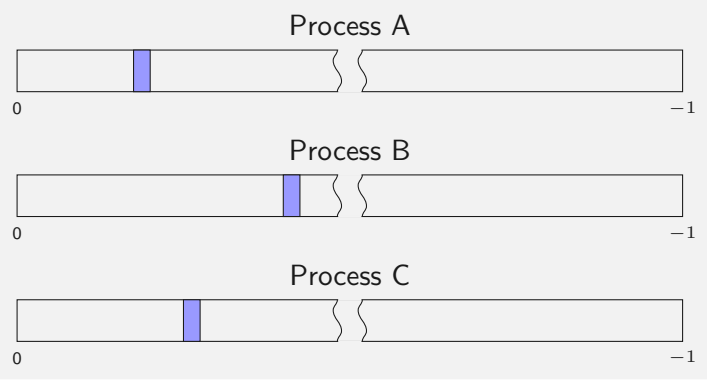
# Address translation on x86-64



# Address Translation Caches



# Address Space Layout Randomization (ASLR)



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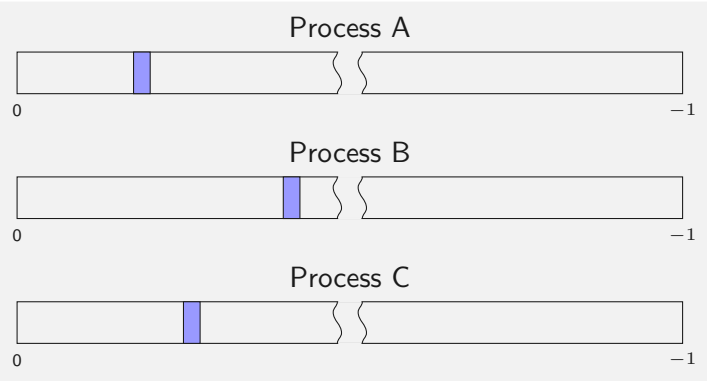
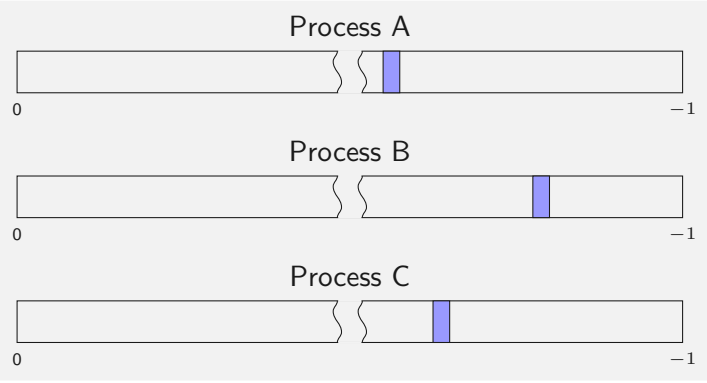



Same library – different offset!

# Kernel Address Space Layout Randomization (KASLR)



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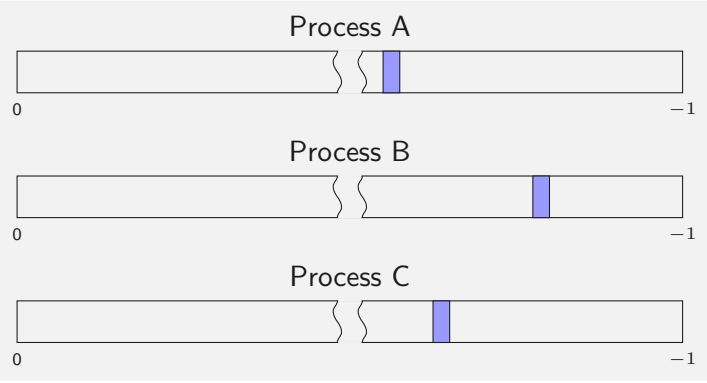
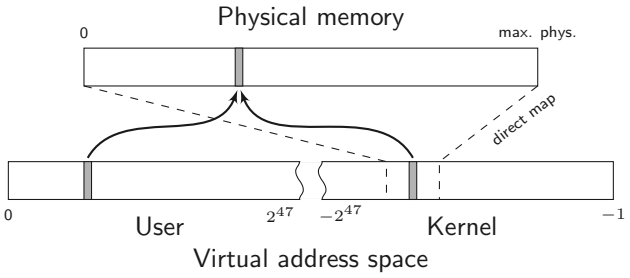



Same driver – different offset!

# Kernel direct-physical map



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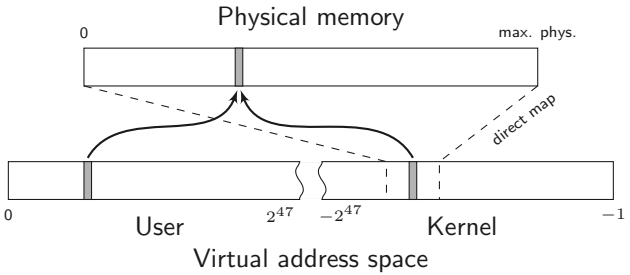
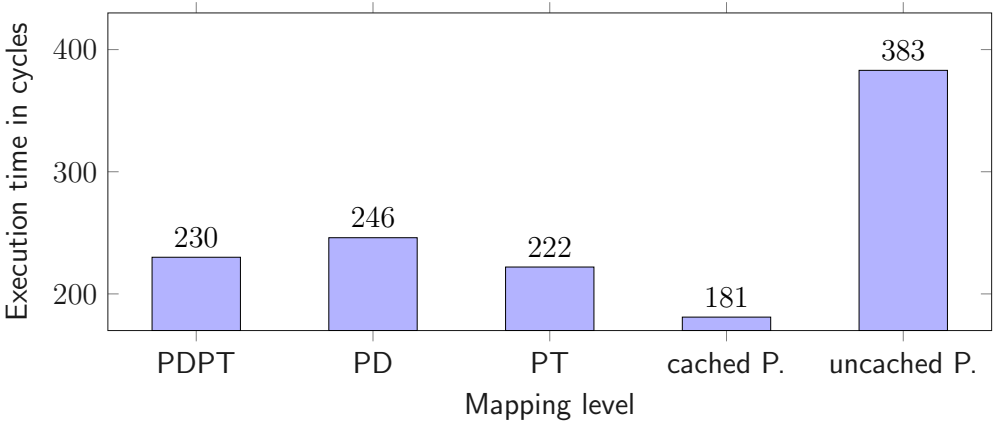
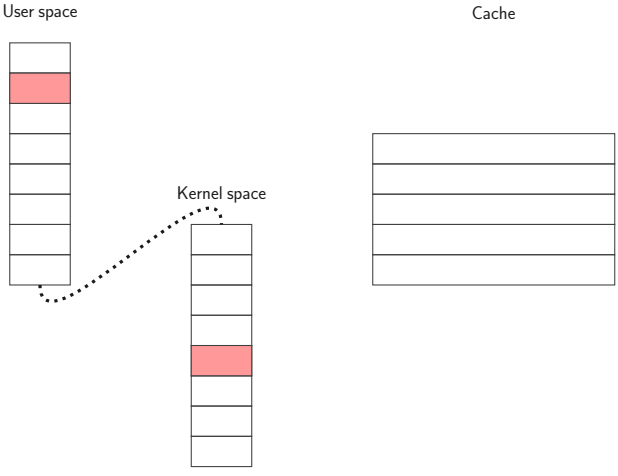



OS X, Linux, BSD, Xen PVM (Amazon EC2)

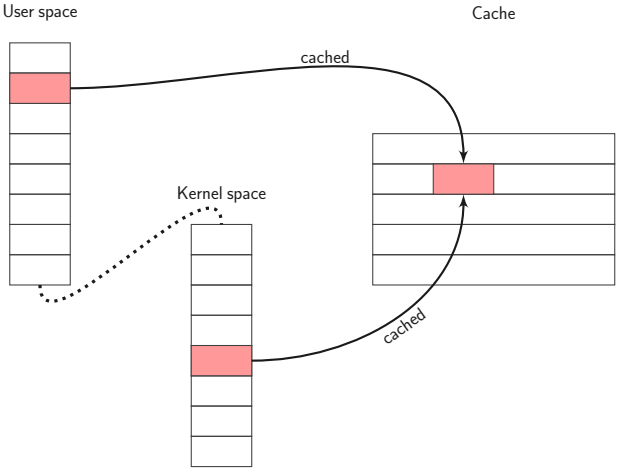
# Translation-Level Oracle



# Address-Translation Oracle



# Address-Translation Oracle



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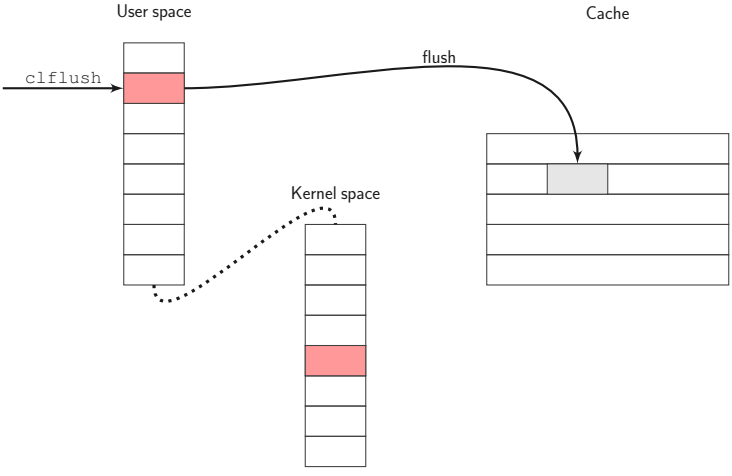

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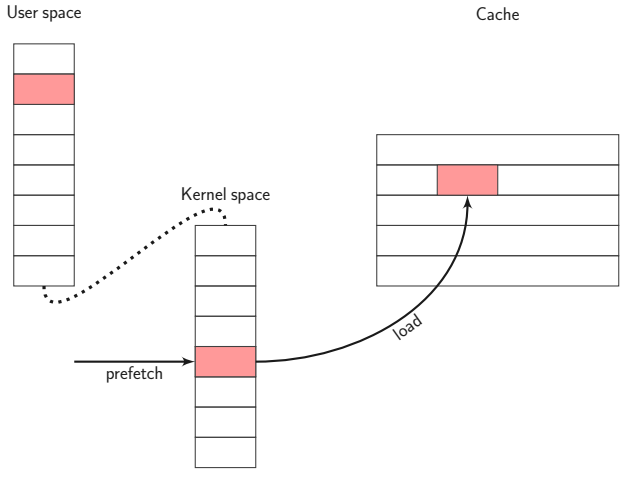
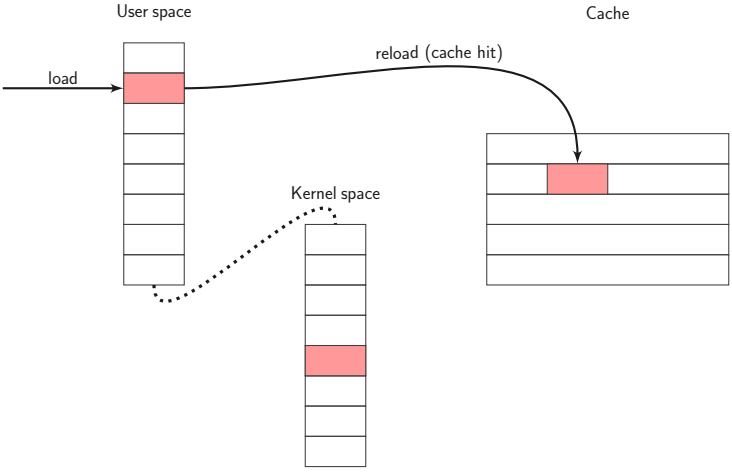
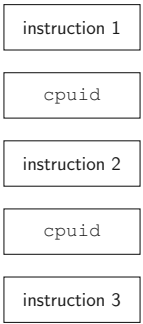


# Address-Translation Oracle



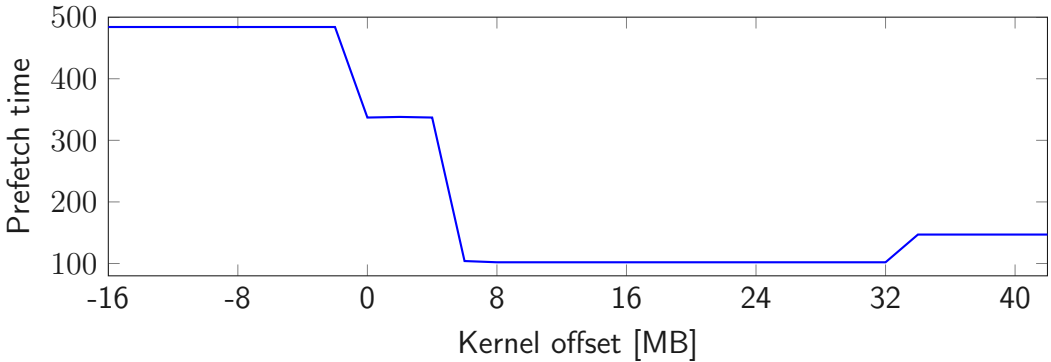
# Timing the prefetch instruction

The CPU may reorder instructions




but not over `cpuid`!

# Breaking KASLR with Prefetch



# Side-Channel Security

## Chapter 2: Cache Template Attacks

**Daniel Gruss**

March 9, 2021

Graz University of Technology

# References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