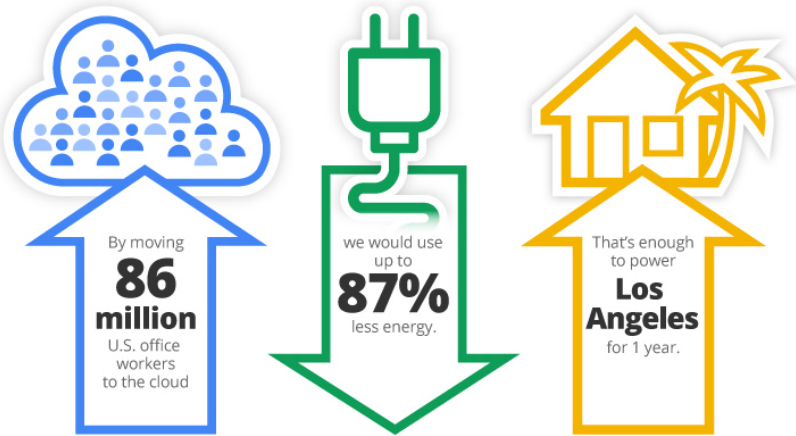
Cloud Operating Systems

Daniel Gruss

2024-03-04

Moving to the cloud can save up to 87% of IT energy



Cloud means Efficiency

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→ Let other processes run in between


IaaS


PaaS


SaaS

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- Isolation of tenants (security, reliability, availability)
- Abstraction of hardware

What is Virtualization?

Virtualization allows to represent resources in a computer in a way they can be used easily and without the need to know details of their properties

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- OS in VM "sees" its hardware, irrespective from the actual hardware in use
- OS does not know if HW is concurrently used by other VMS

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  - multiple servers on one box

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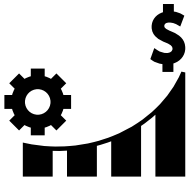

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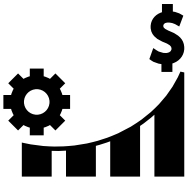

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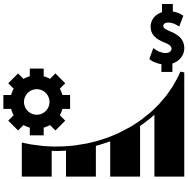

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- simple migration to more powerful hardware

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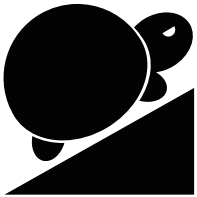

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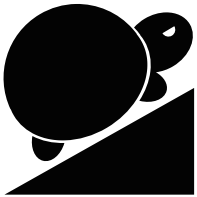

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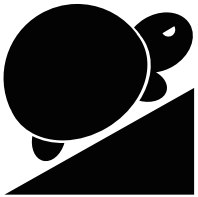

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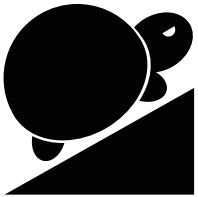

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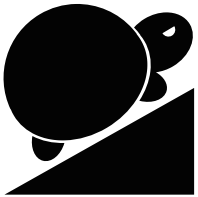

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- Web hosts (FTP access, HTTP website)
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- no hardware support $\rightarrow$ expensive + many problems

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- examples: OpenVZ, Docker, (s)chroot

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- not usable for closed source OSes

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  - every physical component has to be virtualized and requires drivers in OS

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- sets breakpoint and lets OS run

Problems virtualizing on IA-32

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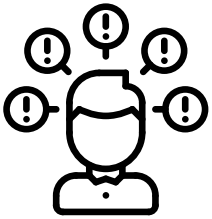

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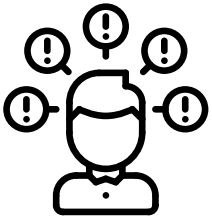

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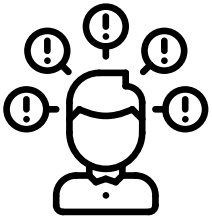

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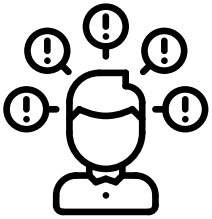

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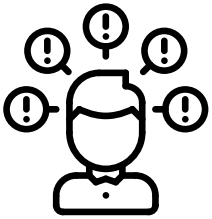

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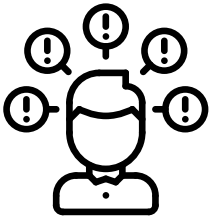

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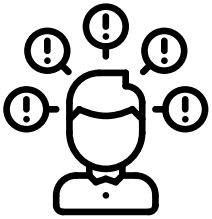

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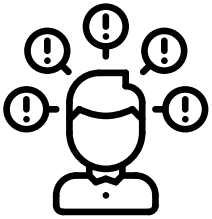

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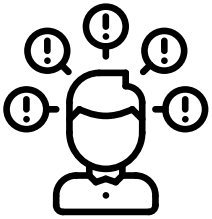

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- Access to these areas not allowed for guest. Invokes switch to hypervisor who has to emulate these accesses

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  - can be executed in any ring without fault (without function)

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- forwarding of virtual interrupts must consider IF

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- cannot be saved and restored when switching between VMs

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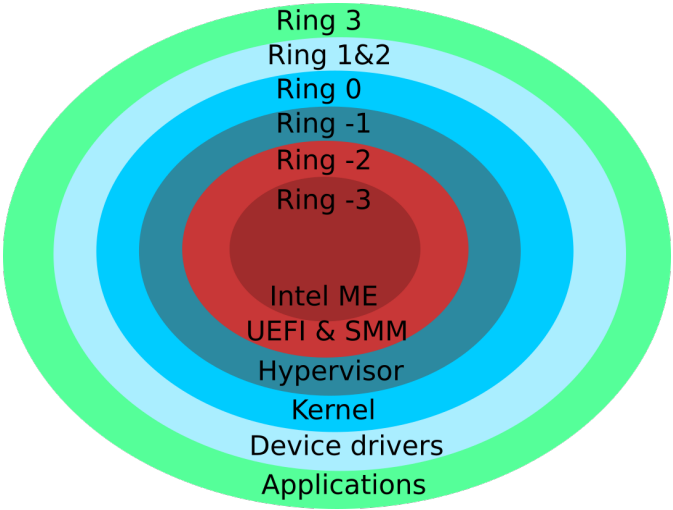
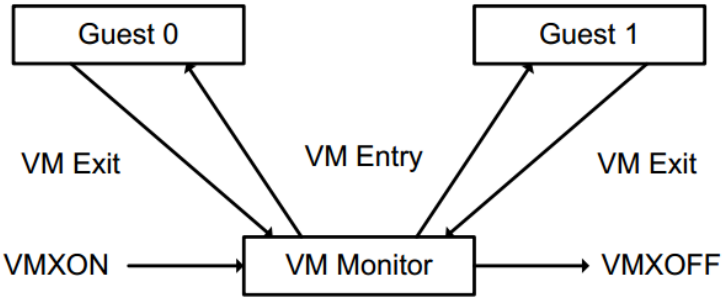
- hypervisor said to be running in “ring -1”

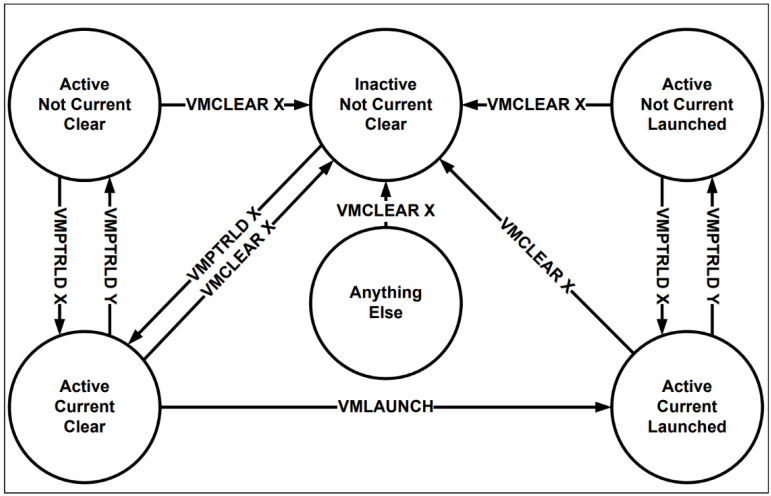
Rings on Intel



VMM Operation



VMM Transitions



- VM entry: root operation $\rightarrow$ non-root operation

VT-x

- VM entry: root operation $\rightarrow$ non-root operation
- VM exit: non-root operation $\rightarrow$ root operation

VT-x

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- VM exit: non-root operation $\rightarrow$ root operation
- VMCS: Virtual Machine Control Structure

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  - Guest-state-area

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VT-x

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- VM exit: non-root operation $\rightarrow$ root operation
- VMCS: Virtual Machine Control Structure
  - Guest-state-area
  - Host-state-area
- Entry/Exit loads/safes information using the proper area

VMCS - Guest State Area

- Contains elements comprising the state of the virtual CPU of a VMCS

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- Contains elements comprising the state of the virtual CPU of a VMCS
- VM-exit requires loading certain registers (like segment registers, CR3, IRTR...)

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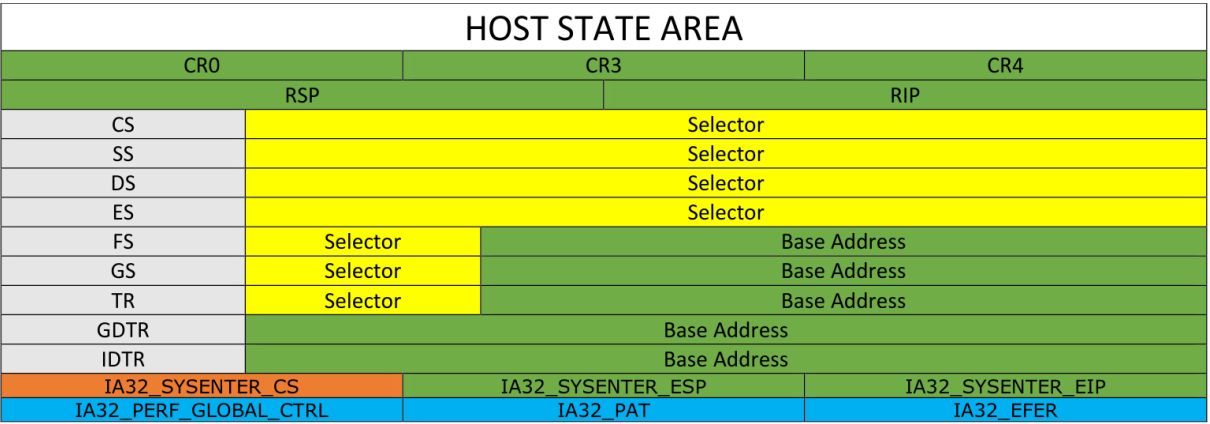
- GSA contains fields for these registers
- GSA contains fields for other information not readable via registers
  - e.g. interruptability state

- Natural-Width fields.
- 16-bits fields.
- 32-bits fields.
- 64-bits fields.

GUEST STATE AREA

CR0	CR3			CR4
DR7				
RSP	RIP			RFLAGS
CS	Selector	Base Address	Segment Limit	Access Right
SS	Selector	Base Address	Segment Limit	Access Right
DS	Selector	Base Address	Segment Limit	Access Right
ES	Selector	Base Address	Segment Limit	Access Right
FS	Selector	Base Address	Segment Limit	Access Right
GS	Selector	Base Address	Segment Limit	Access Right
LDTR	Selector	Base Address	Segment Limit	Access Right
TR	Selector	Base Address	Segment Limit	Access Right
GDTR	Selector	Base Address	Segment Limit	Access Right
IDTR	Selector	Base Address	Segment Limit	Access Right
IA32_DEBUGCTL	IA32_SYSENTER_CS	IA32_SYSENTER_ESP	IA32_SYSENTER_EIP	
IA32_PERF_GLOBAL_CTRL	IA32_PAT	IA32_EFER	IA32_BNDCFGS	
SMBASE				
Activity state	Interruptibility state			
Pending debug exceptions				
VMCS link pointer				
VMX-preemption timer value				
Page-directory-pointer-table entries	PDPTE0	PDPTE1	PDPTE2	PDPTE3
Guest interrupt status				
PML index				


HOST STATE AREA
CR0
CR3
CR4
RSP
RIP
CS
Selector
SS
Selector
DS
Selector
ES
Selector
FS
Selector
Base Address
GS
Selector
Base Address
TR
Selector
Base Address
GDTR
Base Address
IDTR
Base Address
IA32_SYSENTER_CS
IA32_SYSENTER_ESP
IA32_SYSENTER_EIP
IA32_PERF_GLOBAL_CTRL
IA32_PAT
IA32_EFER

- Addressed using physical addresses

VMCS

- Addressed using physical addresses
- not part of guest address space

VMCS

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- not part of guest address space
- hypervisor may run in different address space as guest (CR3 part of state)

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  - exit reason

VMCS

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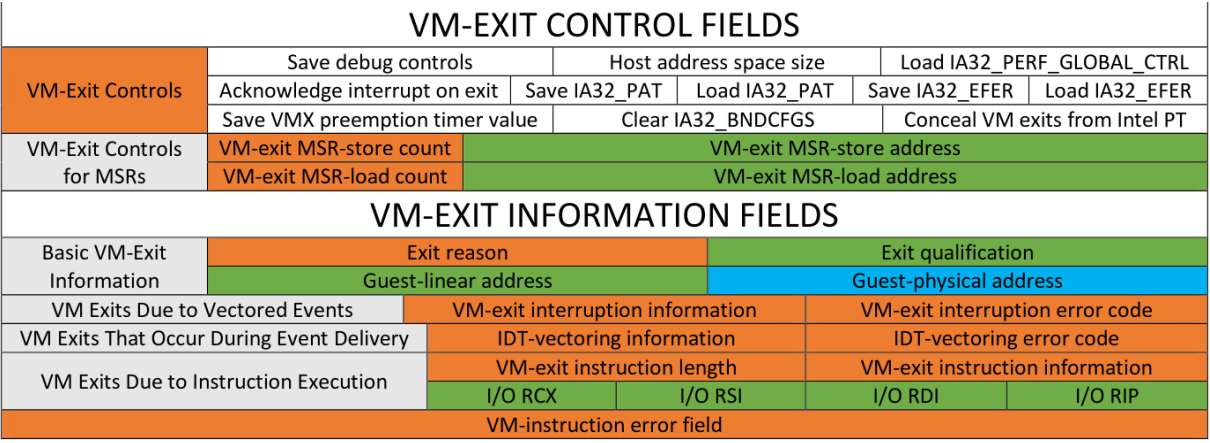
- not part of guest address space
- hypervisor may run in different address space as guest (CR3 part of state)
- VM-exits leave detailed information on reason for exit in VMCS
  - exit reason
  - exit qualification


VM-EXIT CONTROL FIELDS
VM-Exit Controls
Save debug controls
Host address space size
Load IA32_PERF_GLOBAL_CTRL
Acknowledge interrupt on exit
Save IA32_PAT
Load IA32_PAT
Save IA32_EFER
Load IA32_EFER
Save VMX preemption timer value
Clear IA32_BNDCFGS
Conceal VM exits from Intel PT
VM-Exit Controls for MSRs
VM-exit MSR-store count
VM-exit MSR-store address
VM-exit MSR-load count
VM-exit MSR-load address
VM-EXIT INFORMATION FIELDS
Basic VM-Exit Information
Exit reason
Exit qualification
Guest-linear address
Guest-physical address
VM Exits Due to Vectored Events
VM-exit interruption information
VM-exit interruption error code
VM Exits That Occur During Event Delivery
IDT-vectoring information
IDT-vectoring error code
VM Exits Due to Instruction Execution
VM-exit instruction length
VM-exit instruction information
I/O RCX
I/O RSI
I/O RDI
I/O RIP
VM-instruction error field

- Example: MOV CR

- Example: MOV CR
- Exit reason: “control register access”

- Example: MOV CR
- Exit reason: “control register access”
- Exit qualification:

- Example: MOV CR
- Exit reason: “control register access”
- Exit qualification:
  - which CR

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  - which CR
  - direction (Rx→CR or CR→Rx)

- Example: MOV CR
- Exit reason: “control register access”
- Exit qualification:
  - which CR
  - direction (Rx→CR or CR→Rx)
  - register used

CONTROL FIELDS

Pin-Based VM-Execution Controls	External-interrupt exiting	NMI exiting	Virtual NMIs	
	Activate VMX-preemption timer	Process posted interrupts		
Primary processor-based VM-execution controls	Interrupt-window exiting	Use TSC offsetting		
	HLT exiting	INVLPG exiting	MWAIT exiting	RDPMC exiting
	RDTSC exiting	CR3-load exiting	CR3-store exiting	CR8-load exiting
	CR8-store exiting	Use TPR shadow	NMI-window exiting	MOV-DR exiting
	Unconditional I/O exiting	Use I/O bitmaps	Monitor trap flag	Use MSR bitmaps
	MONITOR exiting	PAUSE exiting	Activate secondary controls	
Secondary processor-based VM-execution controls	Virtualize APIC accesses	Enable EPT	Descriptor-table exiting	Enable RDTSCP
	Virtualize x2APIC mode	Enable VPID	WBINVD exiting	Unrestricted guest
	APIC-register virtualization	Virtual-interrupt delivery	PAUSE-loop exiting	
	RDRAND exiting	Enable INVPCID	Enable VM functions	VMCS shadowing
	Enable ENCLS exiting	RDSEED exiting	Enable PML	EPT-violation #VE
	Conceal VMX non-root operation from Intel PT	Enable XSAVES/XRSTORS		
	Mode-based execute control for EPT	Use TSC scaling		
Exception Bitmap	I/O-Bitmap Addresses	TSC-offset		
Guest/Host Masks for CR0	Guest/Host Masks for CR4	Read Shadows for CR0	Read Shadows for CR4	
CR3-target value 0	CR3-target value 1	CR3-target value 2	CR3-target value 3	CR3-target count
APIC Virtualization	APIC-access address	Virtual-APIC address	TPR threshold	
	EOI-exit bitmap 0	EOI-exit bitmap 1	EOI-exit bitmap 2	EOI-exit bitmap 3
	Posted-interrupt notification vector	Posted-interrupt descriptor address		
Read bitmap for low MSRs	Read bitmap for high MSRs	Write bitmap for low MSRs	Write bitmap for low MSRs	
Executive-VMCS Pointer	Extended-Page-Table Pointer	Virtual-Processor Identifier		
PLE_Gap	PLE_Window	VM-function controls	VMREAD bitmap	VMWRITE bitmap
ENCLS-exiting bitmap	PML address			
Virtualization-exception information address	EPTP index	XSS-exiting bitmap		

Virtualization: Trend 2000s $\rightarrow$ 2010s

The next step ($\approx$ 2005):

- Virtualization Hardware Extensions for Intel and AMD

Virtualization: Trend 2000s $\rightarrow$ 2010s

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$\rightarrow$ substantially lower overheads for VMs

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Virtualization: Trend 2000s → 2010s

The next step ($\approx$ 2005):

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→ substantially lower overheads for VMs

→ better isolation

→ IaaS VMs become widely used

Hardware Exentions: Intel VT

- Support for interrupt-virtualization

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- Support for CR0 and CR4-virtualization
  - VM-exit with any change of these registers
  - can be set on which bits this shall happen

Solves our problems

- Address Space Compression

Solves our problems

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  - change of address space with any switch guest/hypervisor

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Solves our problems

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  - change of address space with any switch guest/hypervisor
  - guest owns full virtual address space
- Ring Problems, SYSENTER/SYSEXIT
  - Guest can now run in ring 0

Solves our problems

- Non-faulting Access to Privileged State

Solves our problems

- Non-faulting Access to Privileged State
  - access raise fault into hypervisor

Solves our problems

- Non-faulting Access to Privileged State
  - access raise fault into hypervisor
- Hidden State

Solves our problems

- Non-faulting Access to Privileged State
  - access raise fault into hypervisor
- Hidden State
  - Saved into VMCS

Hypervisor and Virtual Memory

- Hypervisor uses virtual memory

Hypervisor and Virtual Memory

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- guest OS uses virtual memory

Hypervisor and Virtual Memory

- Hypervisor uses virtual memory
- guest OS uses virtual memory
- hardware supports page tables

Hypervisor and Virtual Memory

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- how does this work?

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    - shadow page tables

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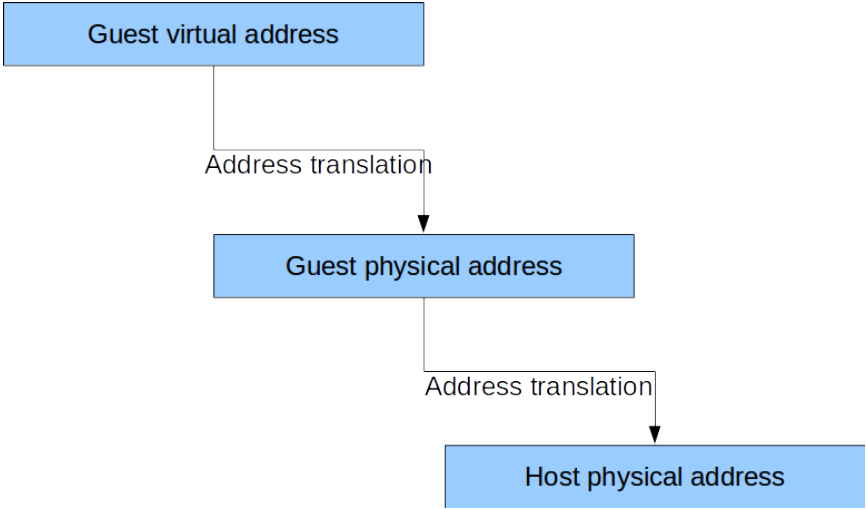
- guest OS uses virtual memory
- hardware supports page tables
- how does this work?
  - shadow page tables
  - hardware support


Guest virtual address
Address translation
Guest physical address
Address translation
Host physical address

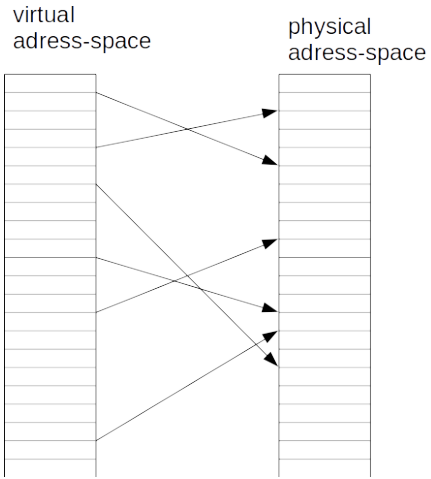
All problems in computer science can be solved by another level of indirection.

All problems in computer science can be solved by another level of indirection.

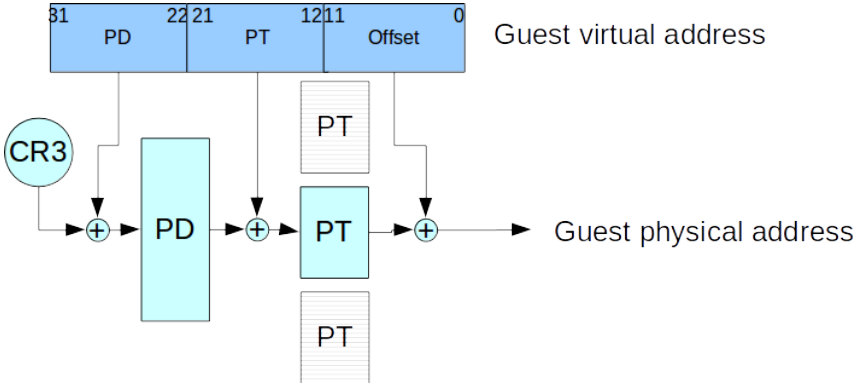
But that usually will create another problem.

David Wheeler

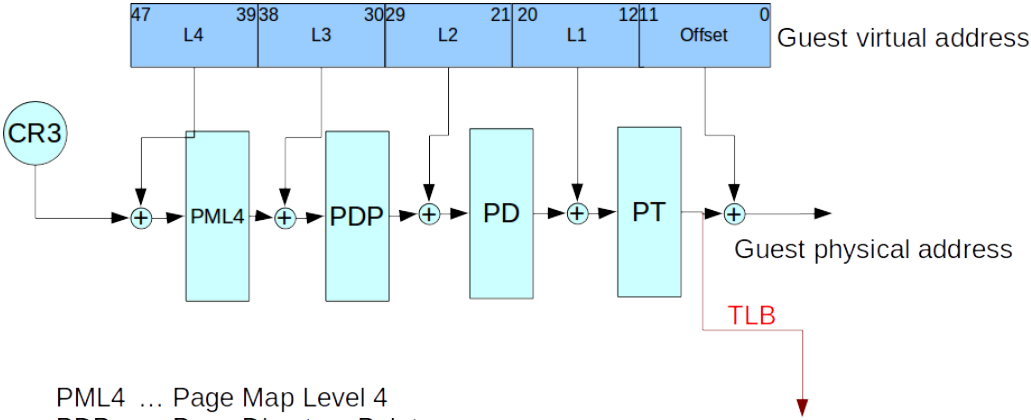
Paging



Known from theory and practice

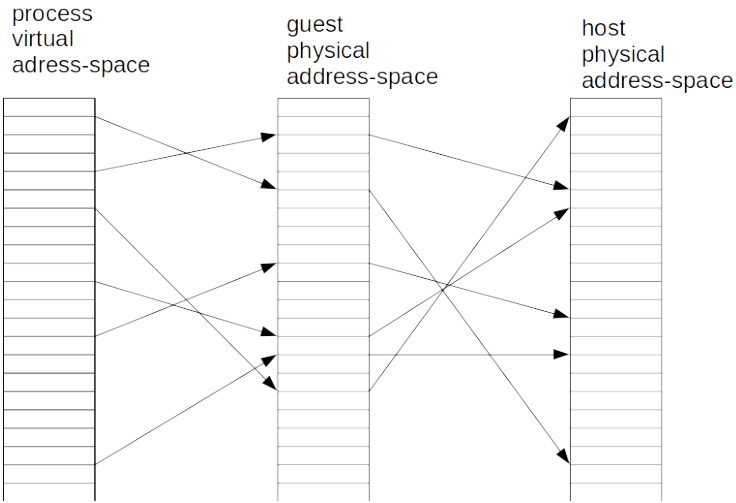


and in 64 bit...

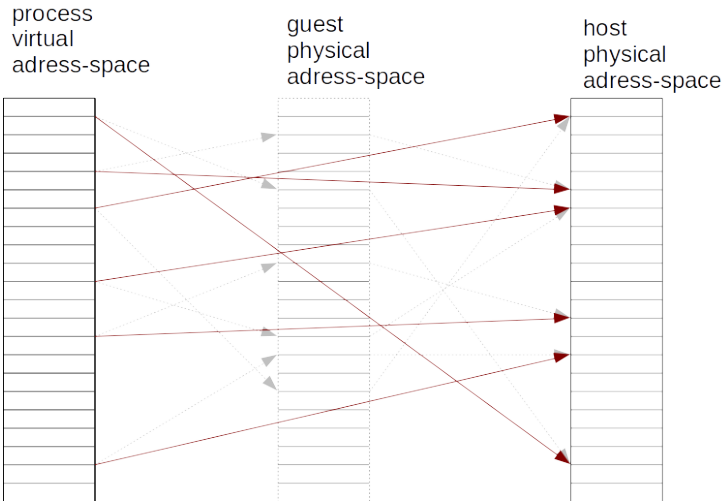


PML4 ... Page Map Level 4
PDP ... Page Directory Pointer
PD ... Page Directory
PT ... Page Table

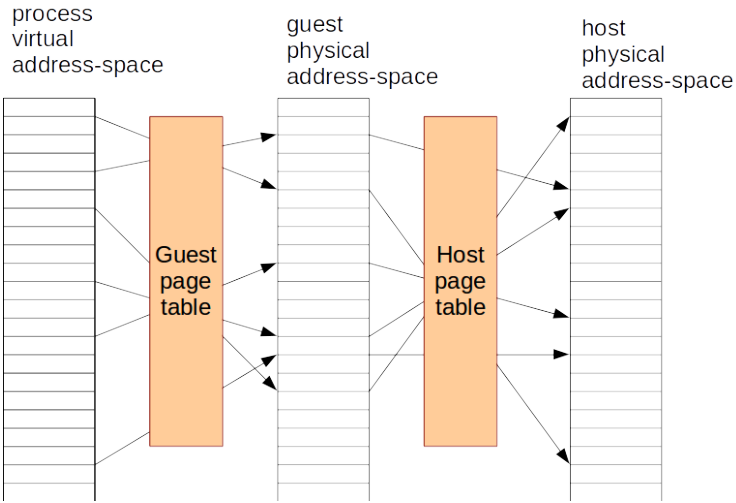
Combined Paging



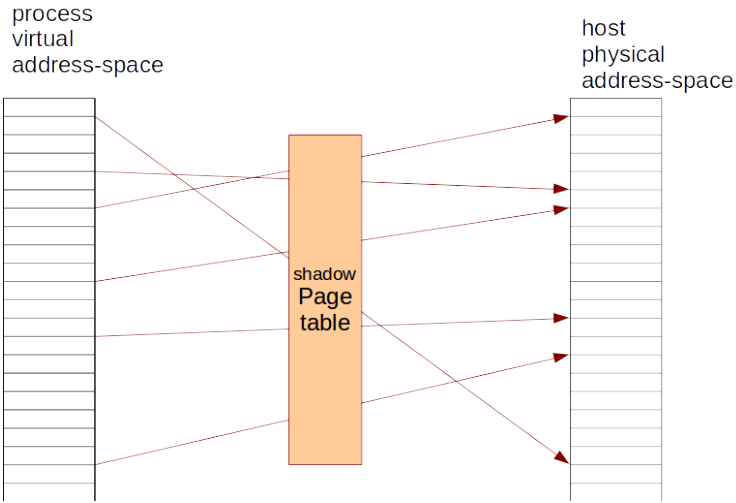
Shadow Page Table



Page Tables


process
virtual
address-space
guest
physical
address-space
host
physical
address-space
Guest
page
table
Host
page
table

Shadow Page Table



Shadow Page Table

- **merges** both page tables into one that the HW uses

Shadow Page Table

- **merges** both page tables into one that the HW uses
- when guest changes own page table

Shadow Page Table

- **merges** both page tables into one that the HW uses
- when guest changes own page table
  - Hypervisor has to catch access

Shadow Page Table

- **merges** both page tables into one that the HW uses
- when guest changes own page table
  - Hypervisor has to catch access
  - update shadow page table

Shadow Page Table

- when HW changes shadow page table

Shadow Page Table

- when HW changes shadow page table
- update guest PT

Shadow Page Table

- when HW changes shadow page table
- update guest PT
  - expensive!

Shadow Page Table

- when HW changes shadow page table
- update guest PT
  - expensive!
  - page faults caught by hypervisor

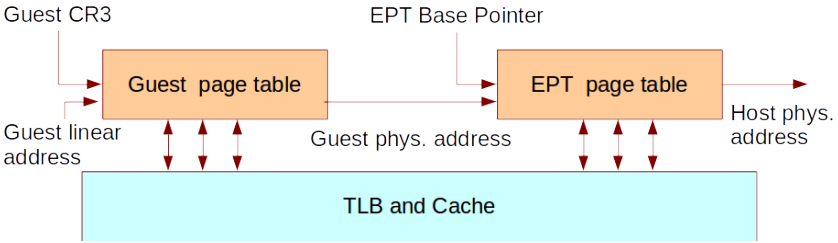
Shadow Page Table

- when HW changes shadow page table
- update guest PT
  - expensive!
  - page faults caught by hypervisor
  - must run through guest PTs

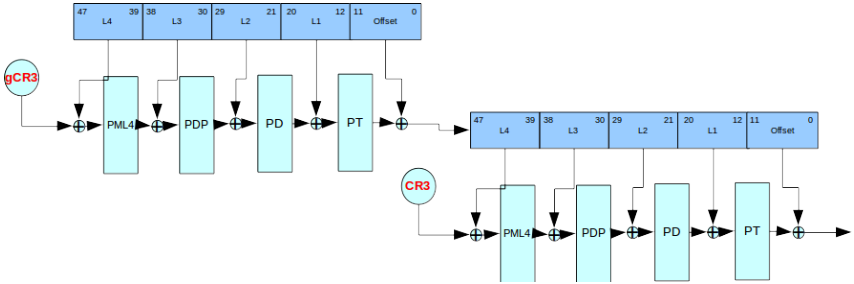
Shadow Page Table

- when HW changes shadow page table
- update guest PT
  - expensive!
  - page faults caught by hypervisor
  - must run through guest PTs
  - must emulate accessed and modified bits for guest

EPT


Guest CR3
EPT Base Pointer
Guest page table
EPT page table
Guest linear address
Guest phys. address
Host phys. address
TLB and Cache

Nested PT (NPT, AMD) / Extended PT (EPT, Intel)



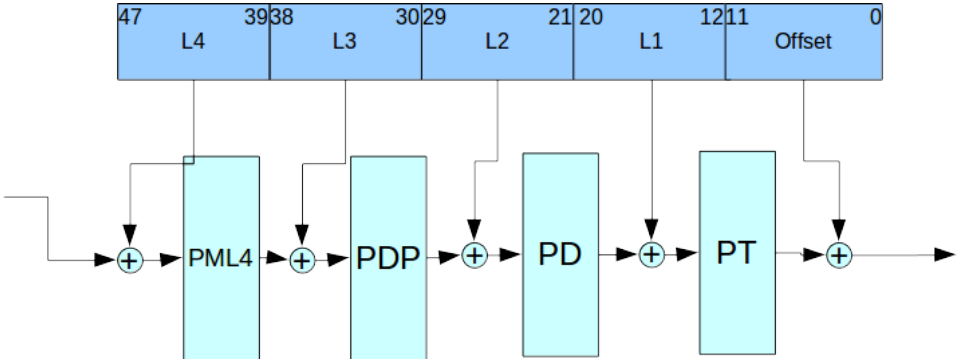
"guest page walk"

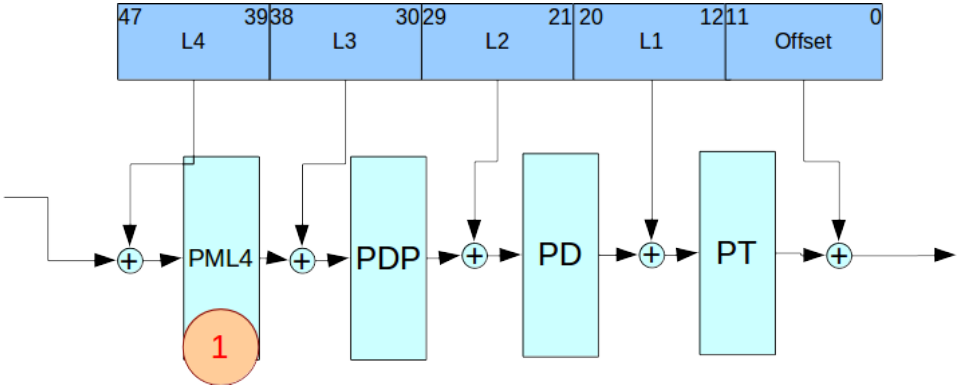
Guest page walk

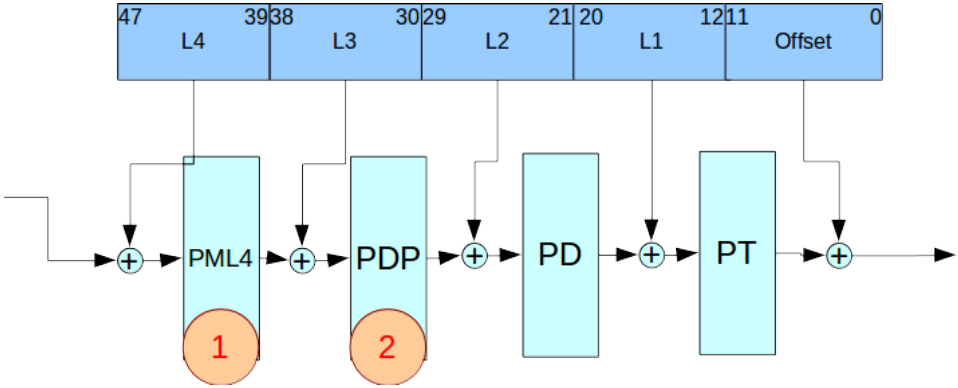
- lots of memory accesses....

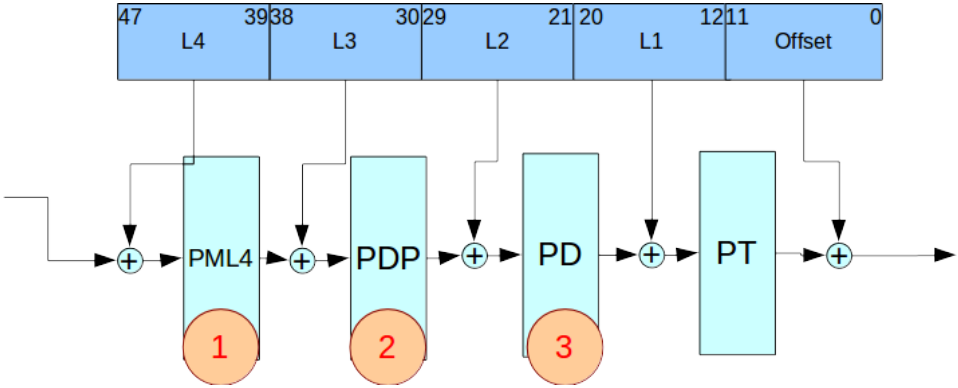
Guest page walk

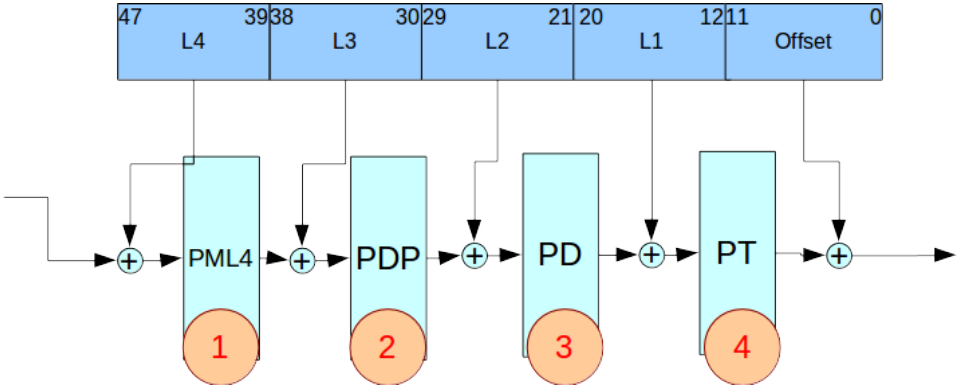
- lots of memory accesses....
- but how many exactly?


47
39
38
30
29
21
20
12
11
0
L4
L3
L2
L1
Offset
PML4
PDP
PD
PT


47
39
L4
38
30
L3
29
21
L2
20
12
L1
11
0
Offset
PML4
PDP
PD
PT
1


47
39
L4
38
30
L3
29
21
L2
20
12
L1
11
0
Offset
PML4
PDP
PD
PT
1
2


47
39
L4
38
30
L3
29
21
L2
20
12
L1
11
0
Offset
PML4
PDP
PD
PT
1
2
3


47
39
38
30
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21
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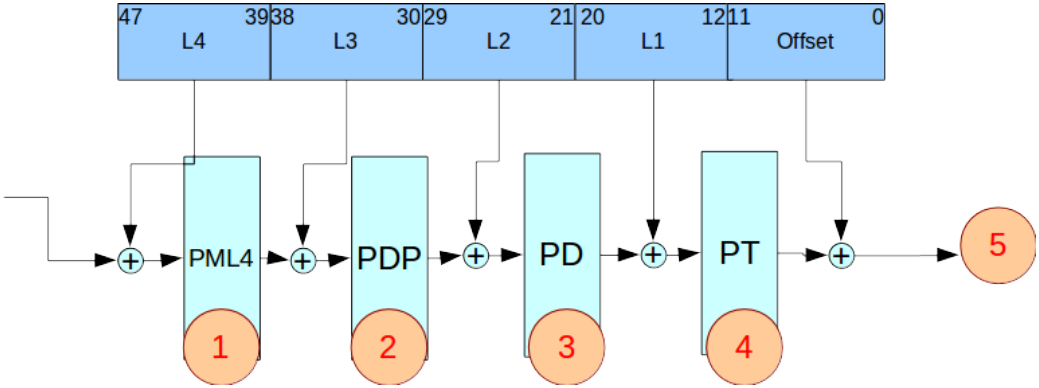
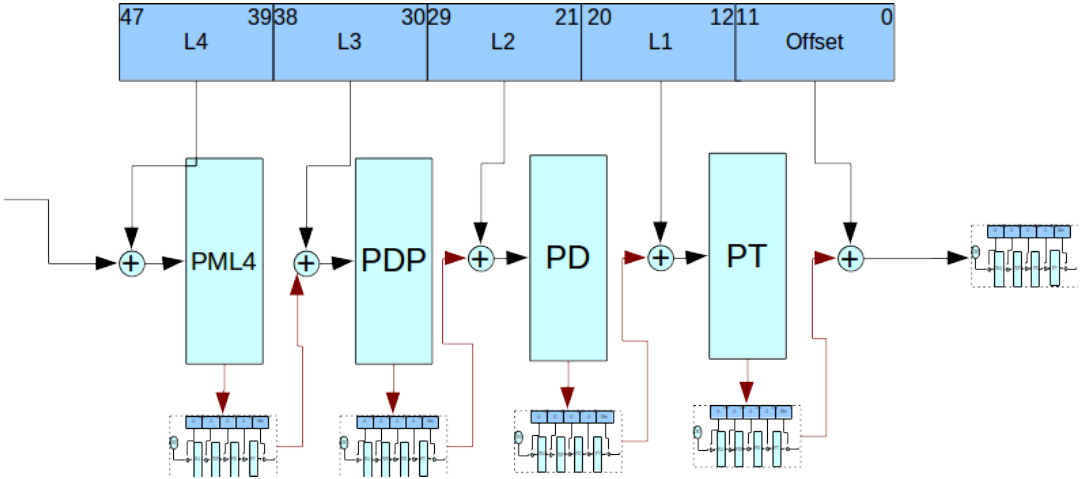
12
11
0
L4
L3
L2
L1
Offset
PML4
PDP
PD
PT
1
2
3
4


47
39
38
30
29
21
20
12
11
0
L4
L3
L2
L1
Offset
PML4
PDP
PD
PT
5
1
2
3
4

And Combined



... and combined ...

max. number of memory accesses per address translation

- 5 on guest level

... and combined ...

max. number of memory accesses per address translation

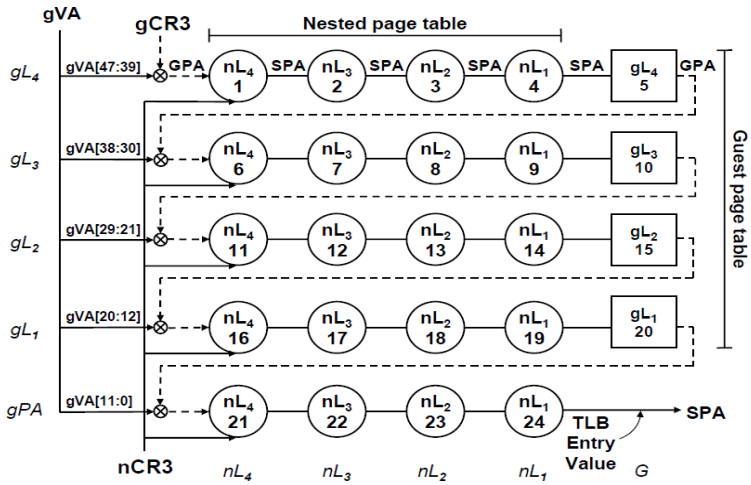
- 5 on guest level
- each induces 5 on host level

... and combined ...

max. number of memory accesses per address translation

- 5 on guest level
- each induces 5 on host level
- makes 25!

Guest Page Walk



Performance

- depending on application: 3.9-4.6 times slower

Performance

- depending on application: 3.9-4.6 times slower
- but: TLB

Intel Features

- EPT only used if VM active

Intel Features

- EPT only used if VM active
- Translations tagged in TLB with EPT base pointer

Intel Features

- EPT only used if VM active
- Translations tagged in TLB with EPT base pointer
  - differentiate TLB-entries of different VMs

Intel Features

- EPT only used if VM active
- Translations tagged in TLB with EPT base pointer
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  - TLB-flush per guest possible

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  - unique value for each VM

Intel Features

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- Translations tagged in TLB with EPT base pointer
  - differentiate TLB-entries of different VMs
  - TLB-flush per guest possible
- VPID: virtual processor ID
  - unique value for each VM
  - translations tagged in TLB using VPID

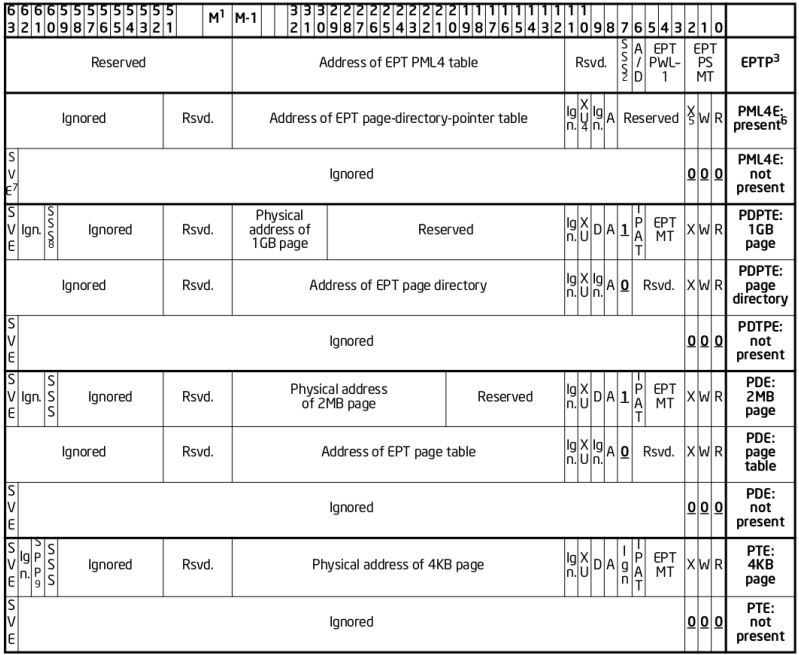

Figure 28-1. Formats of EPTP and EPT Paging-Structure Entries

Setting up a hypervisor

1. Enable VMX via `CR4`

Setting up a hypervisor

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2. Allocate a `VMXON` region and use the `VMXON` instruction

Setting up a hypervisor

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3. Allocate an MSR Bitmap region (we don't want a trap for all MSRs)

Setting up a hypervisor

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4. Use `VMCLEAR` instruction

Setting up a hypervisor

1. Enable VMX via `CR4`
2. Allocate a `VMXON` region and use the `VMXON` instruction
3. Allocate an MSR Bitmap region (we don't want a trap for all MSRs)
4. Use `VMCLEAR` instruction
5. Execute `VMPTRLD` to make a VMCS the "current VMCS"

Setting up a hypervisor

1. Enable VMX via `CR4`
2. Allocate a `VMXON` region and use the `VMXON` instruction
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Virtualization: Trend 2010s $\rightarrow$ 2022+

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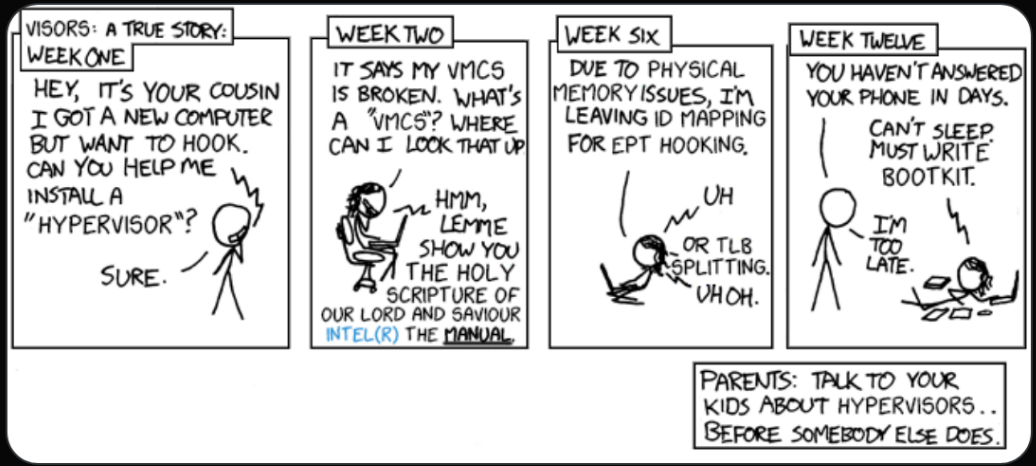
- Context switches between processes are expensive → why not skip process isolation and just use language-level isolation?

This course: hardware-assisted virtualization

Cloud Operating Systems $\rightarrow$ Hardware-assisted virtualization

cts @gf_256 · 5. Apr. 2020

Talk to your kids about hypervisors...before someone else does



19 60

CloudOS: the third time

- Seminar-style

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- You code

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CloudOS: the third time

- Seminar-style
- You code
- You plan
- You present

Team

Fabian Rauscher, Jonas Juffinger, Daniel Gruss

Grading Scale

- 100 P. = 100%

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- 87.5 P. $\rightarrow$ 1

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$\rightarrow$ send us your registration until Monday March 11

Deadlines

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- Grace Period: 48 hours **but no support**

Timeline & Deadlines

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Timeline & Deadlines

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- 14.6. Successful Live Presentation at 21:00, Bonus Points: 5P.