ModelSim

Very good link for installation:

https://profile.iiita.ac.in/bibhas.ghoshal/COA_2020/Lab/ModelSim%20Linux% 20installation.html

Steps:

- 1. Create a project
- 2. Create a new verilog file (sample file attached as adder.v)

Add items to	o the Project ×		
Create New File	Add Existing File		
Create Simulation	Crea File Name	8	
	Add file as type Verilog	Folder-	Browse
	IL	ОК	Cancel

For zooming in I used ctrl+shift+'+'

- 3. Now you can add a testbench file (sample file adder_tb1.v)
- 4. Now go to compile and run compile all option. If everything is correct you will see green ticks in front of the files.
- 5. The go to the Simulate option and run simulate start. If nothing happens, then you need to point it to the simulation file. For this right click in the directory hierarchy display and go to option 'add to the project'. Here select Simulation

configuration and in this window point to the testbench file. Then save this. Then again start the simulation.

Simulation Configuration N	Jame	Add Simulat	ion Configu Place in F Top	uration Folder Level	Add Folder
Design VHDL Verilog	Libraries SDI	Others			< »
▼ Name	Type	Path			
Al work Adder_tb1 fulladder fulladder	Library Module Module Library Library Library Library Library	/home/aikata/Modelsim/worl /home/aikata/Modelsim/add /home/aikata/Modelsim/add \$MODEL_TECH//altera/vhd \$MODEL_TECH//altera/vhd \$MODEL_TECH//altera/vhd \$MODEL_TECH//altera/vhd	c er_tb1.v /220model og/220m /altera /altera_in og/altera /altera_mf		X
Design Unit(s) work.adder_	tb1				default -
					Save

6. Now the simulation will start but an empty wave with objects on the right.



7. To this add the signals and then in the Simulate option go to Run>Run-all. Now you should be able to see the simulated waves.

