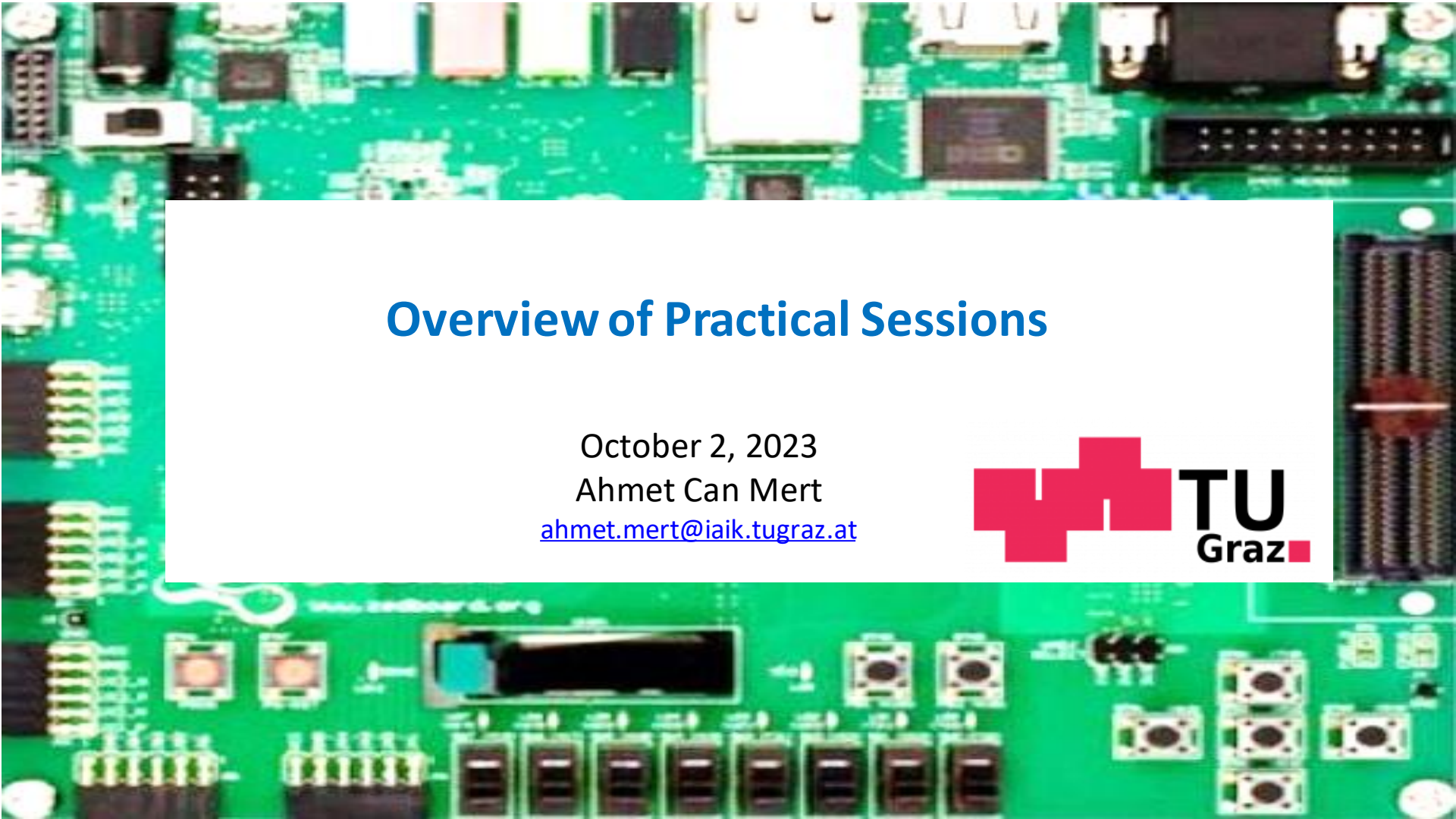

Overview of Practical Sessions

October 2, 2023

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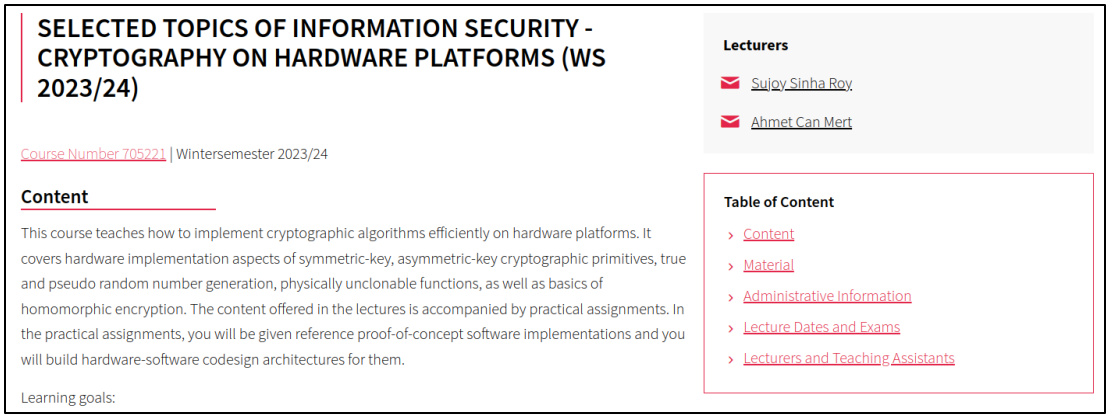
TU Graz

A High-level Overview

- We have one-hour practical session every week (Tuesday, 10:00-11:00). We will use it for ...
  - Tutorials
    - Verilog, Software tool, FPGA
  - Explaining assignments
  - Office hour and Q&A

Course webpage/Discord Channel

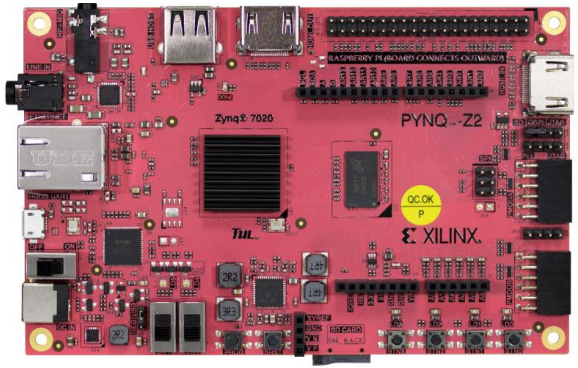
- All course materials (lecture slides, tutorials, assignments...) will be available in course webpage.
  - https://www.iaik.tugraz.at/chw

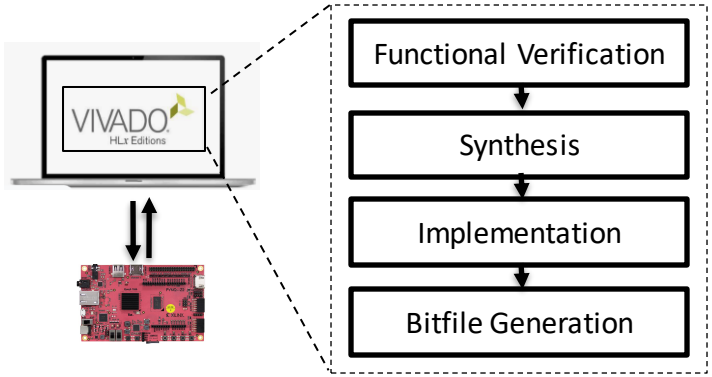


- Discord Channel
  - Announcements, Q&A, ...
  - Link (also in the course webpage): https://discord.gg/hNe9mjeZH

Tools: FPGA Board

- For some parts of the assignments, we will use the PYNQ-Z2 FPGA board for implementing the cryptographic primitives.
  - Artix-7 FPGA equipped with ARM Cortex-A9 FPGA





- Collect your board from our office (room IF02024) once you form your group
  - One FPGA per group

Tools: Software

- In the assignments, we will use Xilinx tools for RTL simulation and FPGA programming.
  - Xilinx Vivado 2019.1 Webpack -> Xilinx Vitis
  - For RTL simulation, you are free to use other tools (i.e., Modelsim).
    (We recommend Xilinx Vivado/Vitis)

- Installation guide will be available in course webpage.
  - Windows and Ubuntu
  - No support for MACOS
    (We recommend Windows OS)

Tools: Hardware Description Languages (HDLs)

- In this course, we will use Verilog for assignments.
  - SystemVerilog is also fine
  - VHDL?

- Tomorrow, we will continue with a quick Verilog recap.

Assignments

- There will be two assignments.
  - HW design and writing its Verilog code
  - RTL-level simulation/verification
  - Verification on actual FPGA

- **100% of your grade is from assignments.**