Operating Systems

Virtual Memory Basics

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Address Translation

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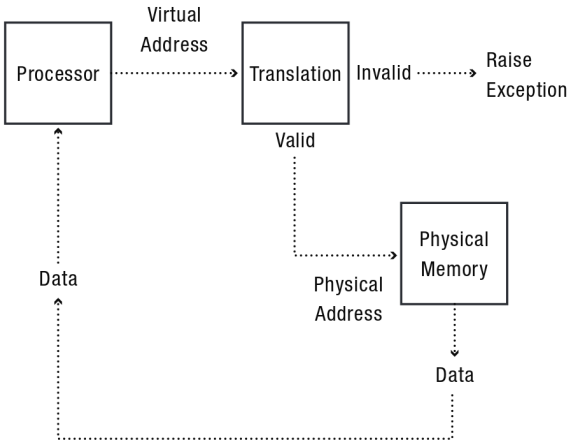
- programmers perspective:
  - pointers point to objects etc.
  - transparent: it is not necessary to know how memory reference is converted to data

Address Translation - Idea / Overview



Address Translation Concepts

- Memory protection

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  - Shared libraries, interprocess communication
- Sparse address space
  - Multiple regions for dynamic allocation (heaps/stacks)

Address Translation Concepts

- Efficiency

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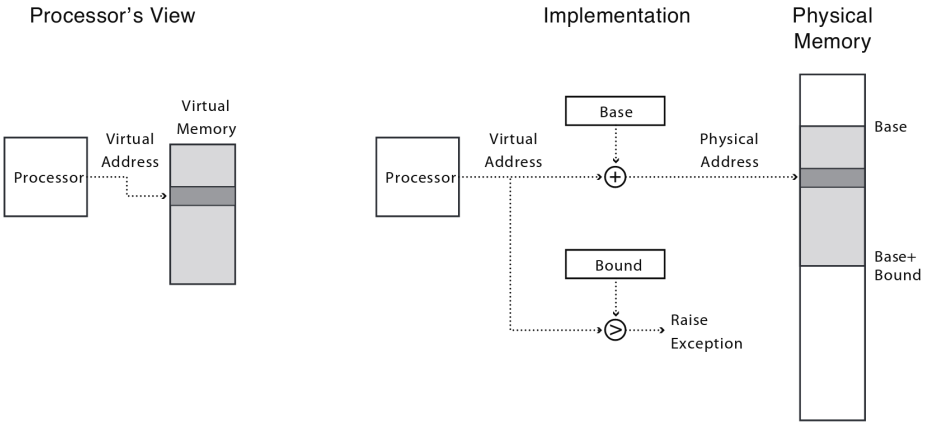
- Portability

Base-Limit or Base and bounds



Virtually Addressed Base and Bounds

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Segmentation

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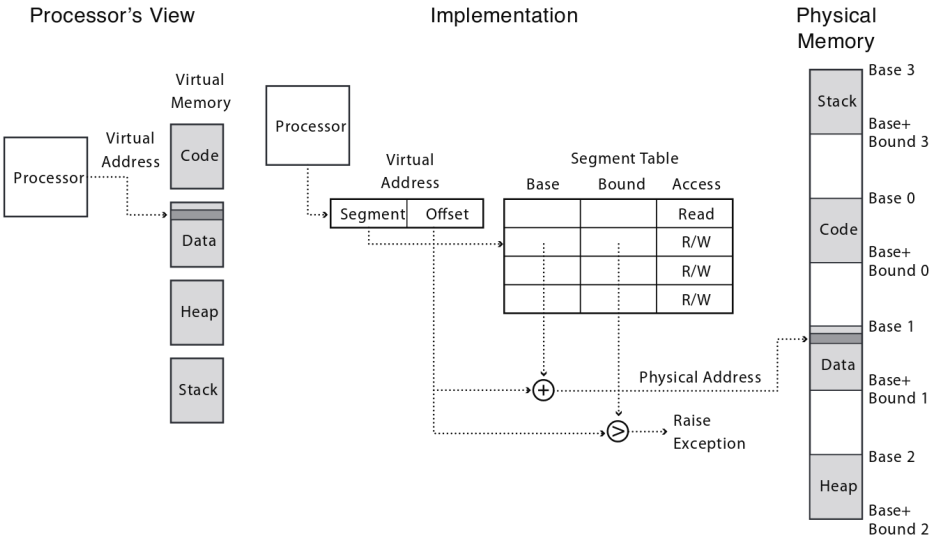
- Each entry controls a portion of the virtual address space

Segmentation



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  - Each segment has: start, length, access permission

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  - correct programs will not generate references outside valid memory
  - trying to read or write data that does not exist: bug-indication

Shared Memory

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$\rightarrow$ set segment read only

Fork and Copy on Write

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- make a copy of the segment and resume

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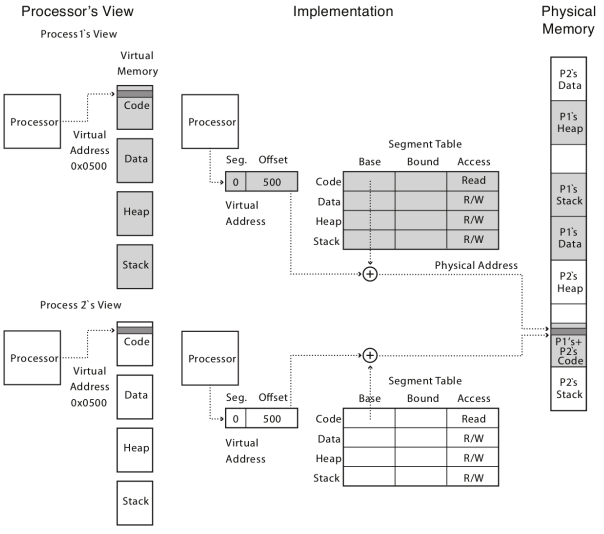

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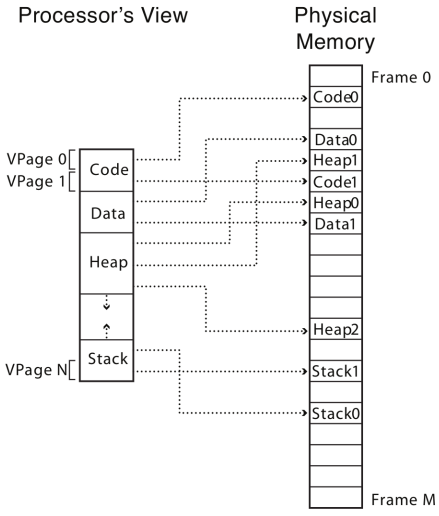
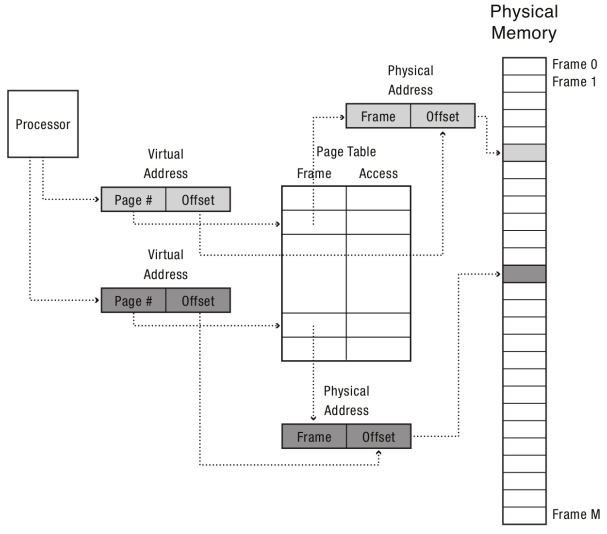
Logical View of Page Table Address Translation



paging - implementation



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  - Internal fragmentation: if we don't need all of the space inside a fixed size chunk

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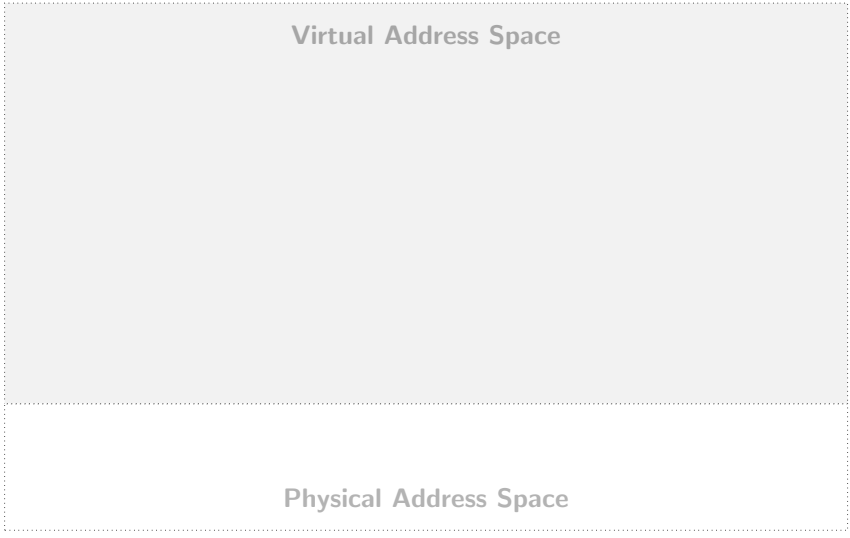
  - Set entries in both page tables to the same physical page number
  - Need core map of physical page numbers to track which processes are pointing to which physical page numbers (e.g. *reference count*)

Copy-on-Write on Unix/Linux



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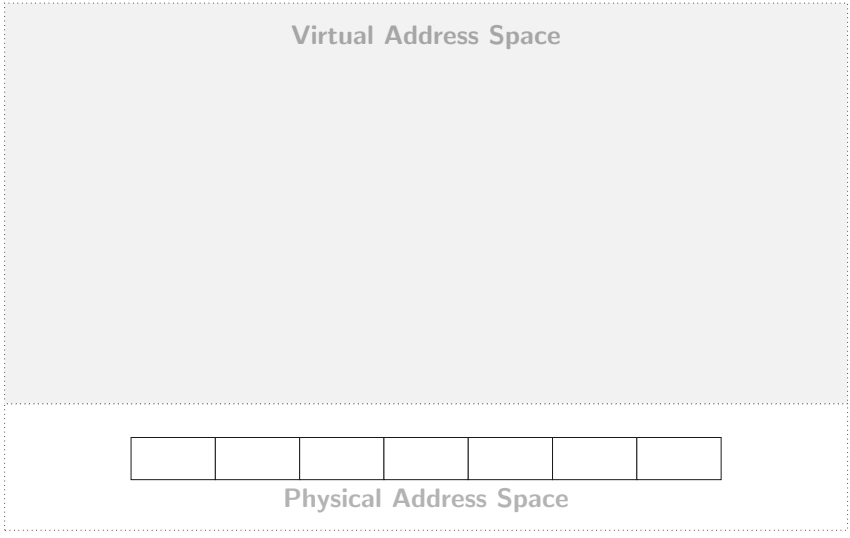

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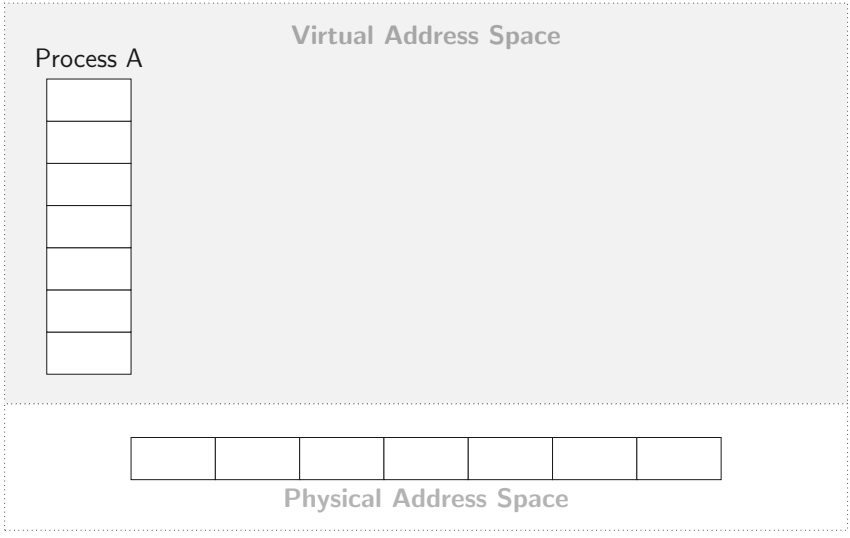

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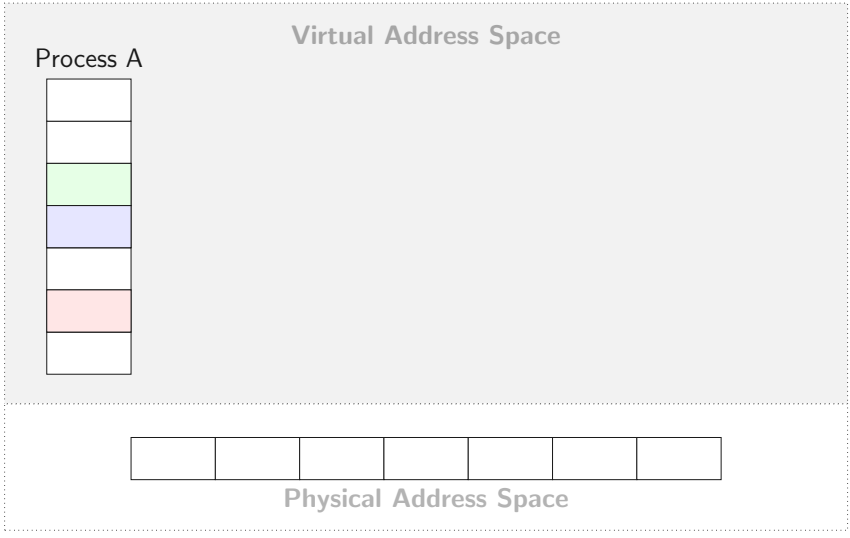

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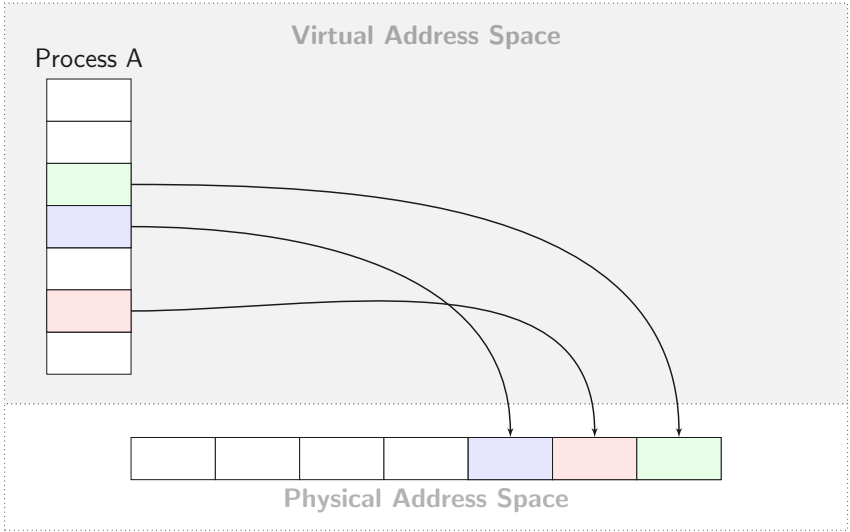

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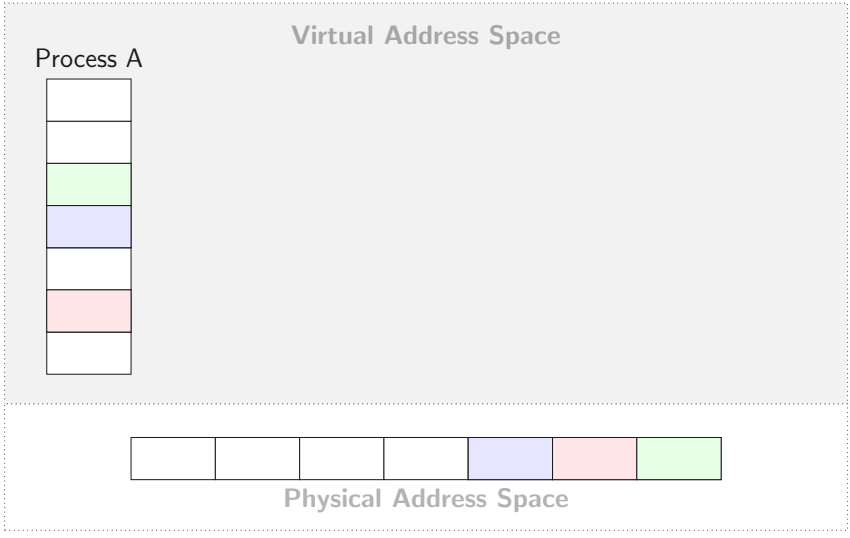

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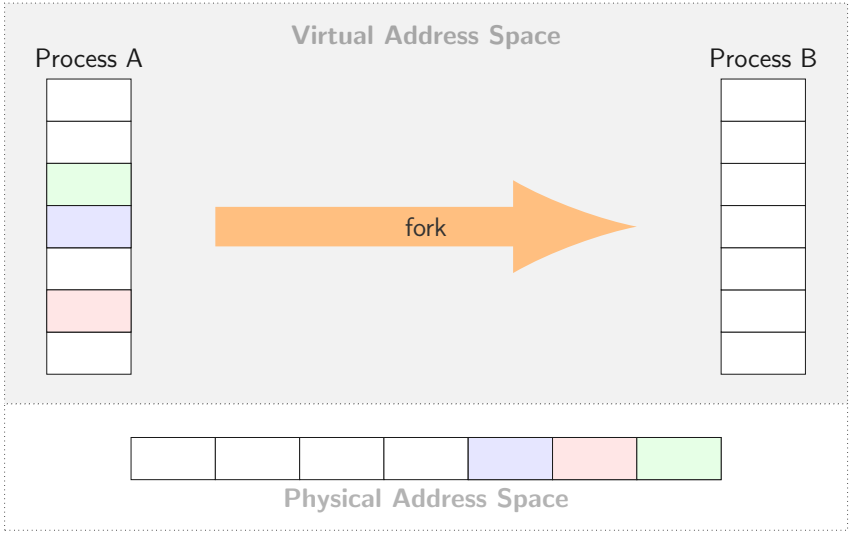

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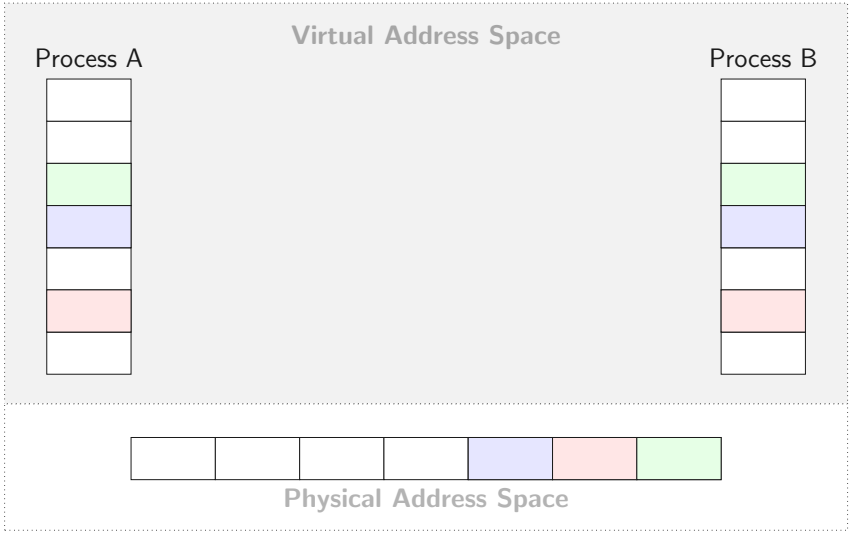

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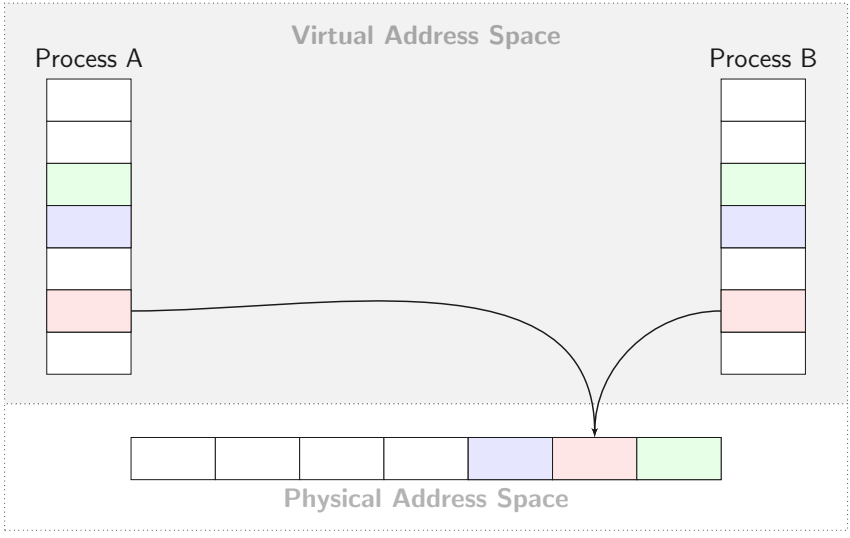

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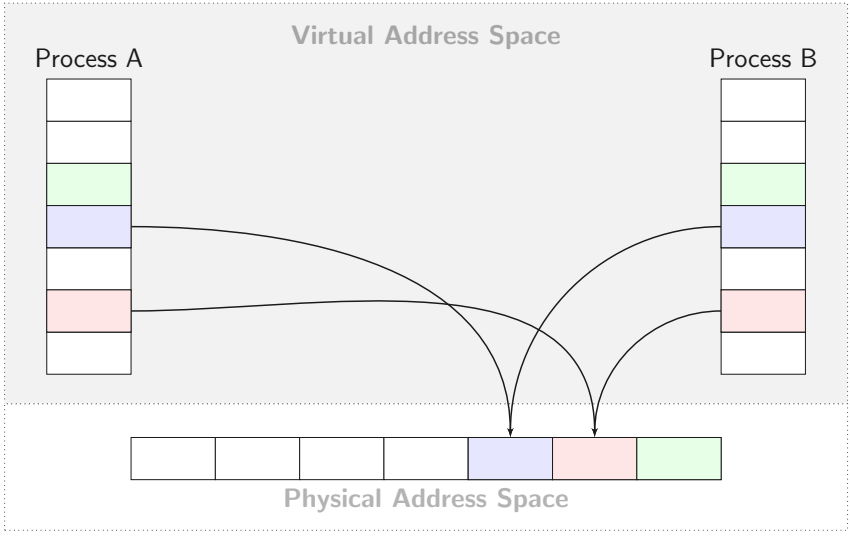

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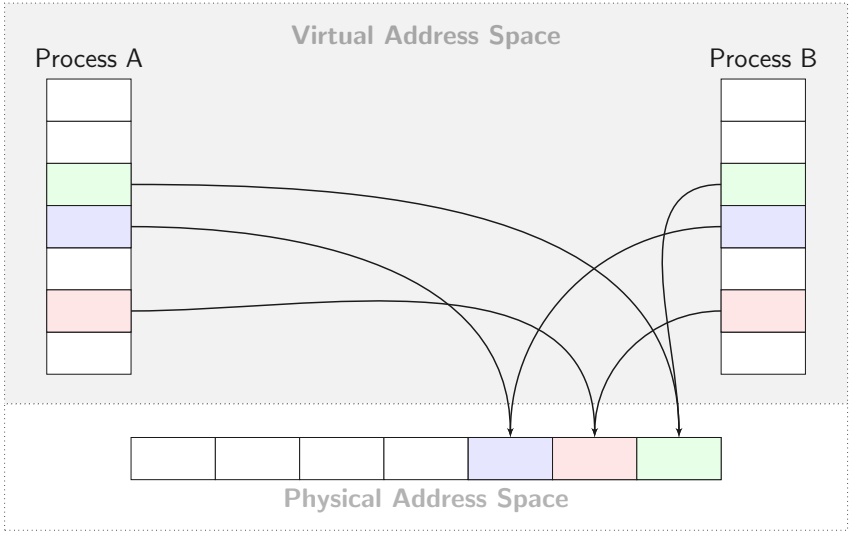

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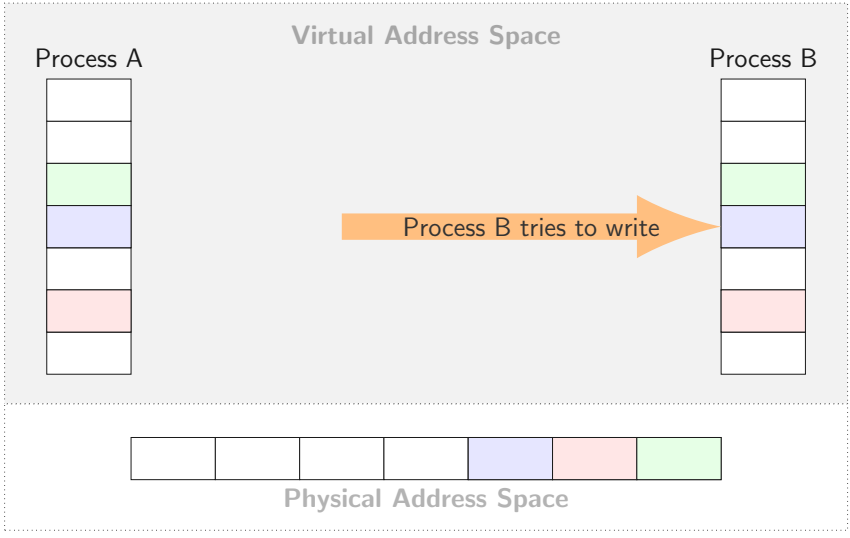

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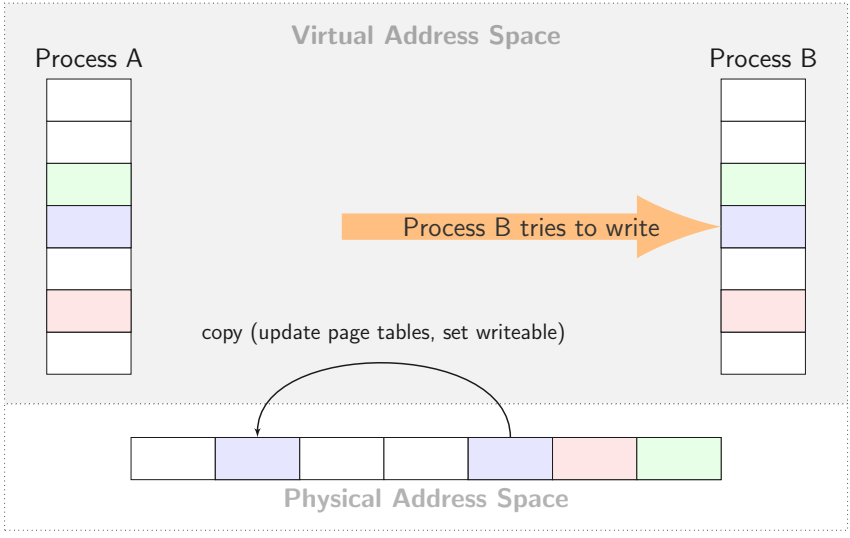

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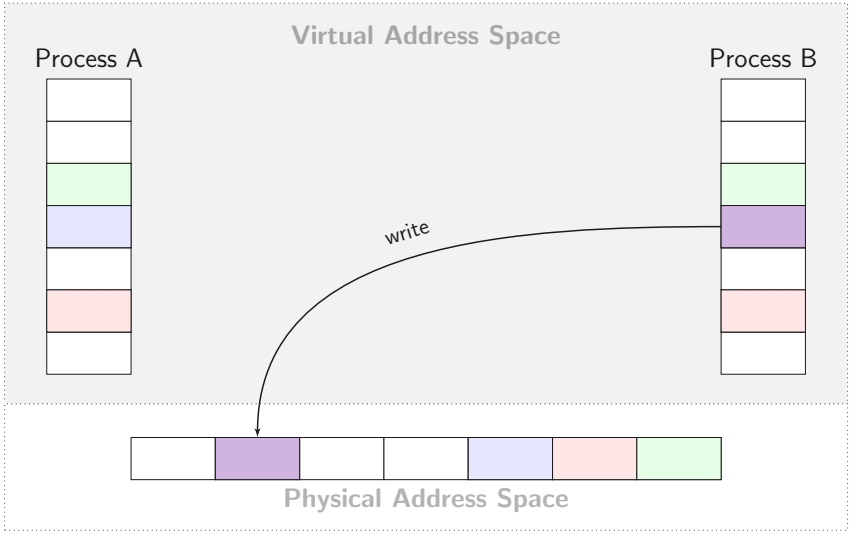

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  - Remaining pages can be transferred in the background while program is running

Scheduling a Process (with Demand Paging)

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- The principle of locality ensures that

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$\rightarrow$ may lower page fault frequency

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  - 64-bits $\rightarrow$ 4 quadrillion page table entries

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  - Efficient disk transfers (fixed size units, page size multiple of disk sector)

Multi-level Translation

- Fixed-size page as lowest level unit of allocation
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  - Fine granularity for protection/sharing

Paged Segmentation

- Process memory is segmented

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- Segment table entry:

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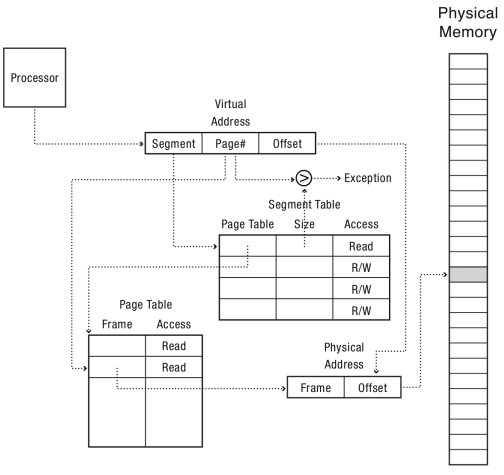
- Process memory is segmented
- Segment table entry:
  - Pointer to page table
  - Page table length (# of pages in segment)
  - Access permissions
- Page table entry:
  - Physical page number
  - Access permissions
- Share/protection at either page or segment-level

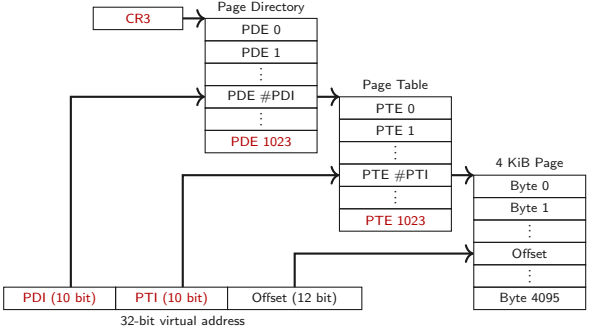
Paged Segmentation



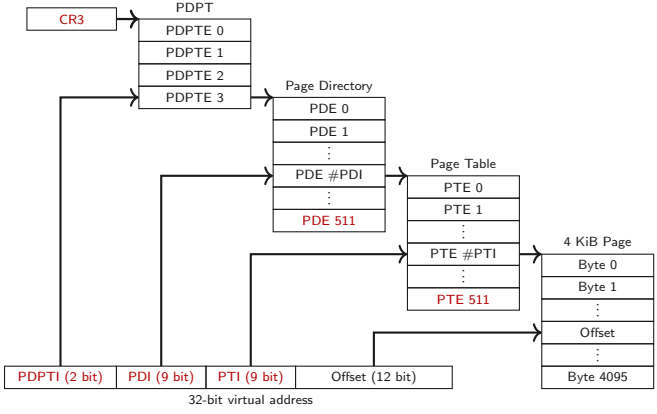
Question

- With paged segmentation, what must be saved/restored across a process context switch?

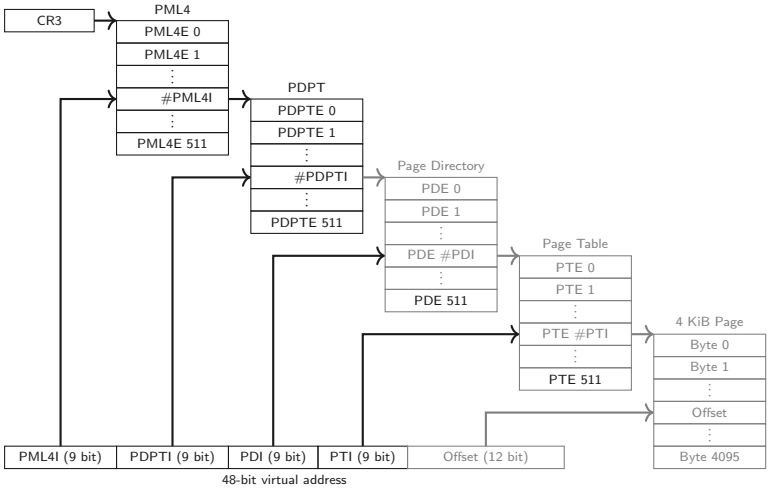
Paging: x86-32 with page size 4 KiB



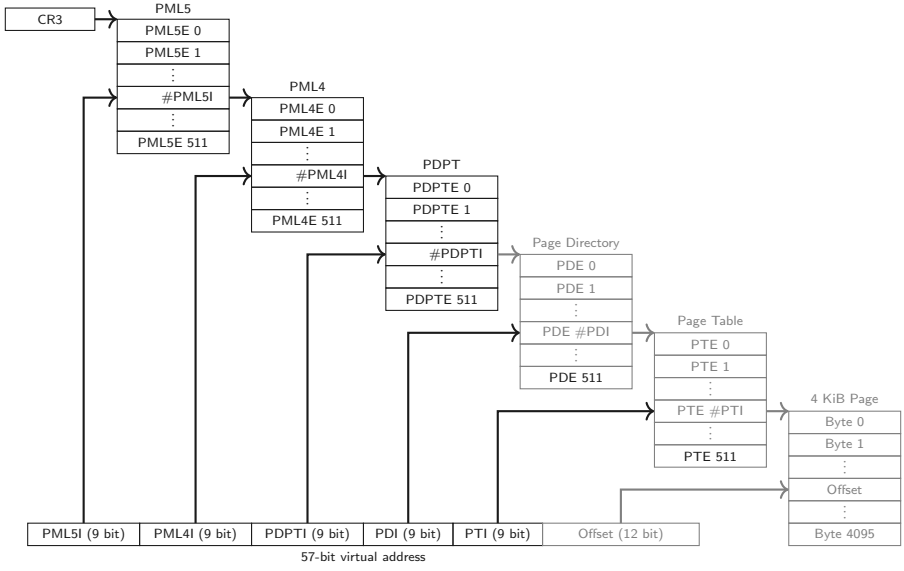
Paging: x86-32-PAE with page size 4 KiB



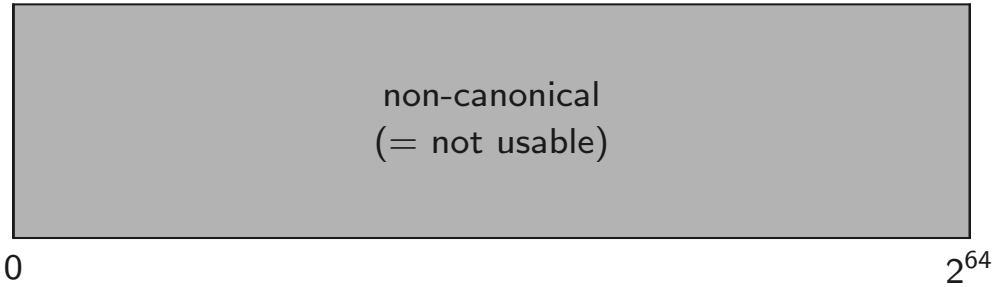
Paging: x86-64 with page size 4 KiB



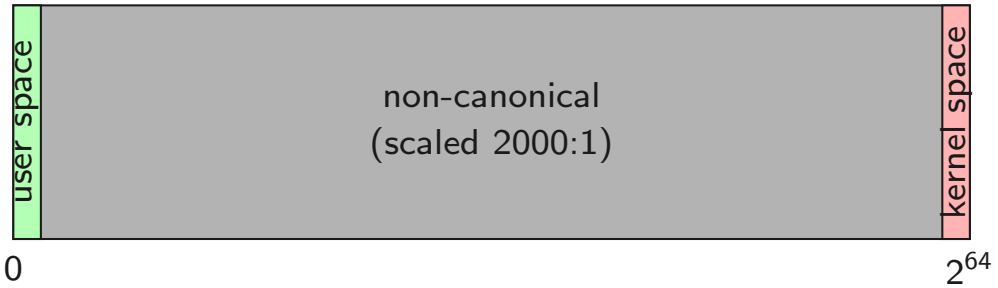
Paging: x86-64 with PML5 and page size 4 KiB



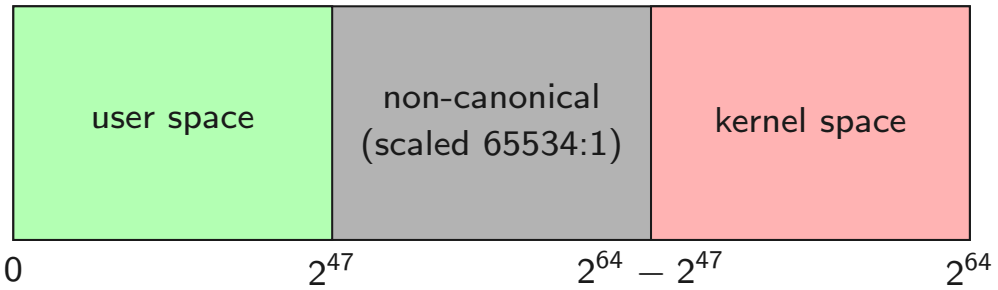
x86-64 Memory Layout (with PML4)



x86-64 Memory Layout (with PML4, scaled)



x86-64 Memory Layout (with PML4, scaled)



Address Translation on x86 processors

Intel Pentium

- Segmentation and paging

Intel Pentium

- Segmentation and paging
- 16 K segments, each 4 GB

Intel Pentium

- Segmentation and paging
- 16 K segments, each 4 GB
  - Few segments

Intel Pentium

- Segmentation and paging
- 16 K segments, each 4 GB
  - Few segments
  - Large segments

LDT - GDT

- Local Descriptor Table LDT

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  - local segments (Code, Data, Stack)

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  - for system segments

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  - local segments (Code, Data, Stack)
- Global Descriptor Table GDT
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  - also for kernel

Segment Registers

- 6 segment registers

Segment Registers

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  - CS: Selector for Code Segment

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  - GS: Selector for Data Segment
  - SS: Selector for Stack Segment

Segment Selector

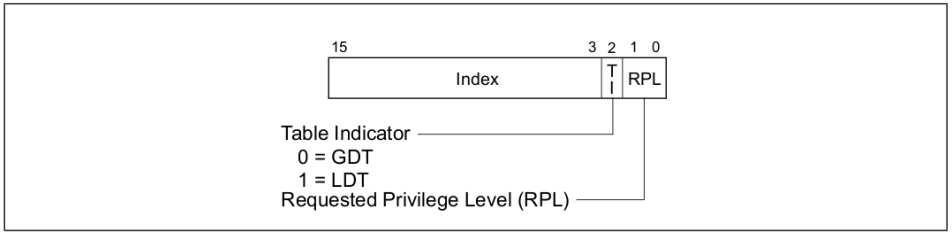


Figure 3-6. Segment Selector

Segment Selector

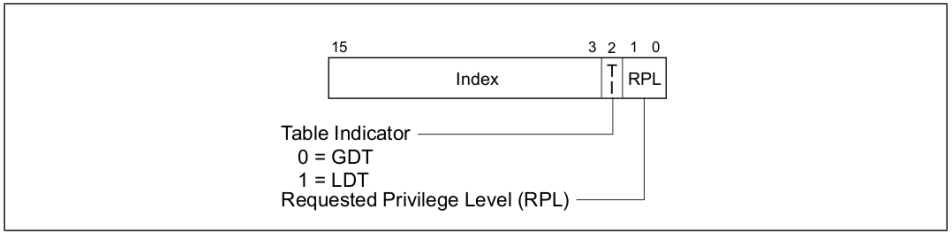


Figure 3-6. Segment Selector

- Null Segment at index 0 → cannot be used

Segment Selector

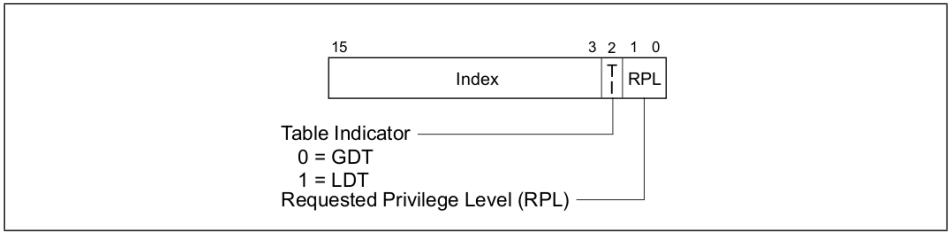


Figure 3-6. Segment Selector

- Null Segment at index 0 → cannot be used
- Modifying a segment register loads corresponding descriptor into an internal CPU register

Hidden Part of Segment Registers

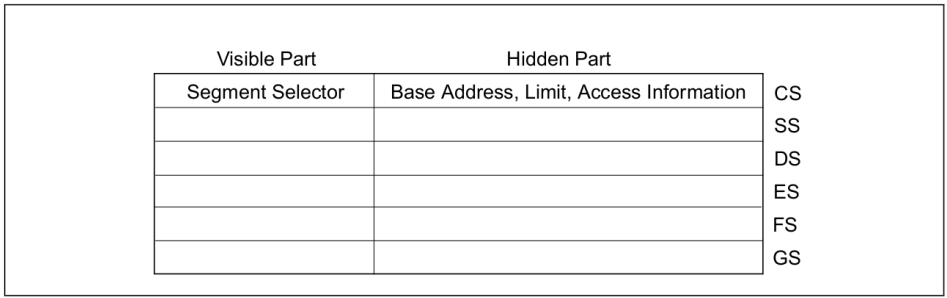
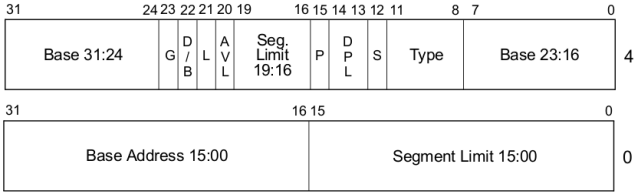


Figure 3-7. Segment Registers

Segment Descriptor



L — 64-bit code segment (IA-32e mode only)
AVL — Available for use by system software
BASE — Segment base address
D/B — Default operation size (0 = 16-bit segment; 1 = 32-bit segment)
DPL — Descriptor privilege level
G — Granularity
LIMIT — Segment Limit
P — Segment present
S — Descriptor type (0 = system; 1 = code or data)
TYPE — Segment type

Figure 3-8. Segment Descriptor

Address translation

- we start with (selector, offset)

Address translation

- we start with (selector, offset)
- CPU looks for correct descriptor in internal registers

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  - check limits of course
- result: linear address
- paging turned off: linear address is physical address

Address translation

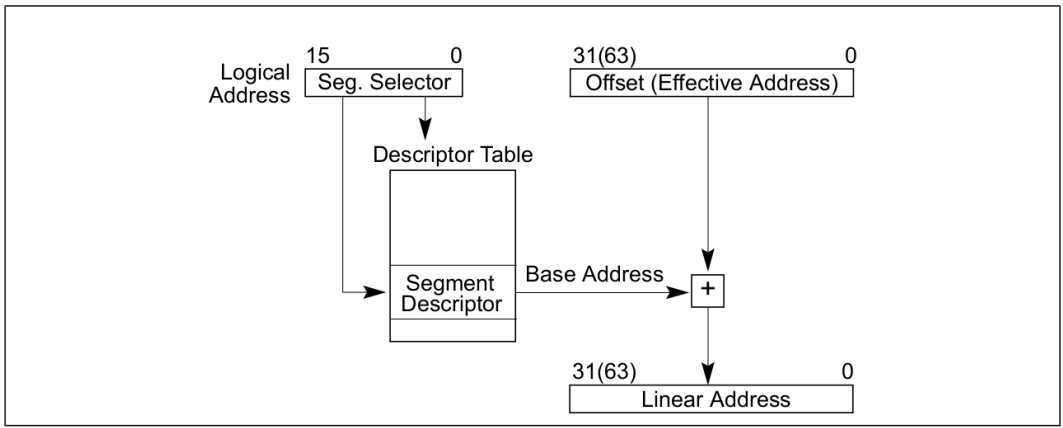


Figure 3-5. Logical Address to Linear Address Translation

Combining Segments and Paging

OSes today have only a very small number of segments:

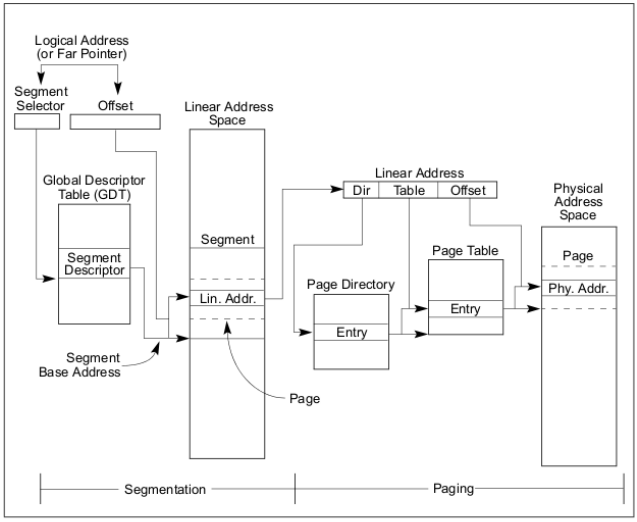
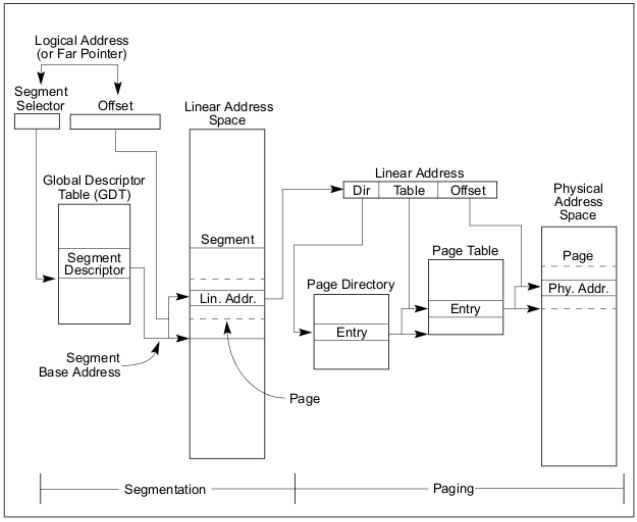


Figure 3-1. Segmentation and Paging

Combining Segments and Paging

OSes today have only a very small number of segments:

- 1 for user code



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Combining Segments and Paging

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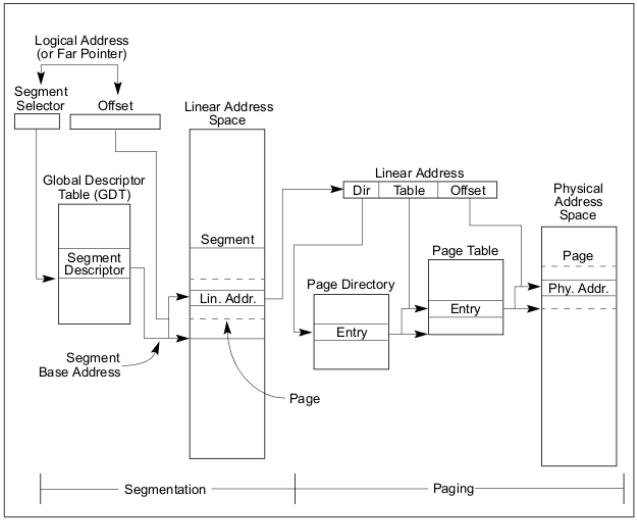

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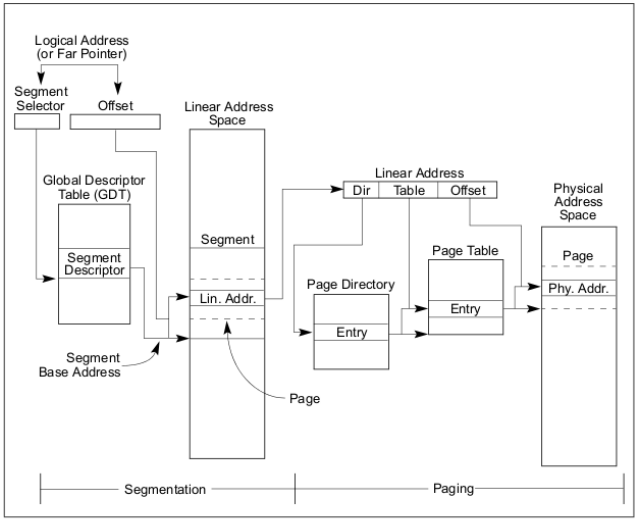

Figure 3-1. Segmentation and Paging

Combining Segments and Paging

OSes today have only a very small number of segments:

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- 1 for user data
- 1 for user thread local storage
- 1 for kernel code

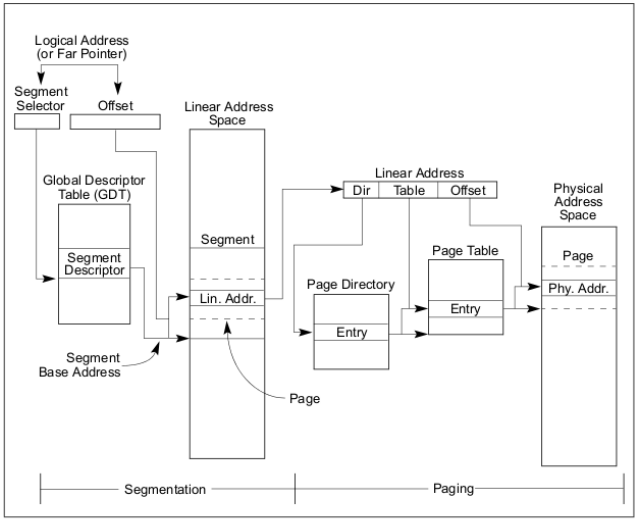

Figure 3-1. Segmentation and Paging

Combining Segments and Paging

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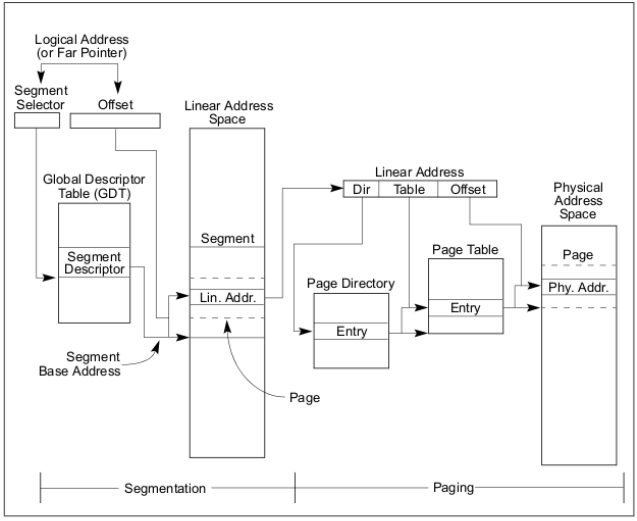

Figure 3-1. Segmentation and Paging

Combining Segments and Paging

OSes today have only a very small number of segments:

- 1 for user code
- 1 for user data
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- 1 for kernel code
- 1 for kernel data
- 1 for kernel core local storage

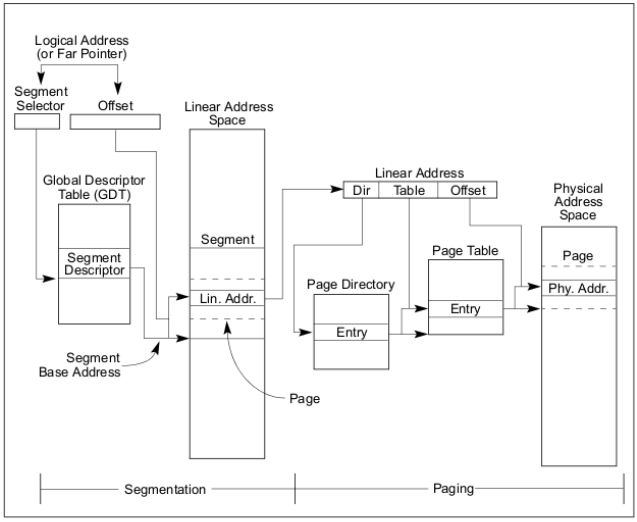

Figure 3-1. Segmentation and Paging

Segments Today

- x86-64 requires segment base to be 0 and limit to be unlimited

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- not even used anymore to separate code and data

Segments Today

- x86-64 requires segment base to be 0 and limit to be unlimited
- not even used anymore to separate code and data
- most OSes today only use segments to determine the privilege level

Take Aways

Virtual memory

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Virtual memory

- is based on Segmentation and Paging

Take Aways

Virtual memory

- is based on Segmentation and Paging
- enables effective protection mechanisms

Take Aways

Virtual memory

- is based on Segmentation and Paging
- enables effective protection mechanisms
-

Take Aways

Virtual memory

- is based on Segmentation and Paging
- enables effective protection mechanisms
-
- enables sparse address spaces