

The use of examination aids (e.g., calculators) is prohibited. Answers can be given in German or English. Please refrain from using lead pencils and red ink pens.

Grading scale: 00–25: insufficient 26–31: sufficient 32–38: satisfactory
39–44: good 45–50: very good

Q1. (10 points) **SystemVerilog Finite State Machine:**

- (a) An incomplete timing diagram can be found on the next page. Complete the missing signals in the diagram. Use binary encoding for signal values.
- (b) Draw the ASM diagram for this finite-state machine.
- (c) The table on the right specifies the output logic. Specify the logical formulas for two output signals.
- (d) What kind of FSM is given? What is the name of the other type of finite-state machines and explain the difference. Change one line of the truth table to create the other type of FSM.

state_p		in_i	out_o	
[1]	[0]		[1]	[0]
0	0	0	1	1
0	0	1	1	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	0

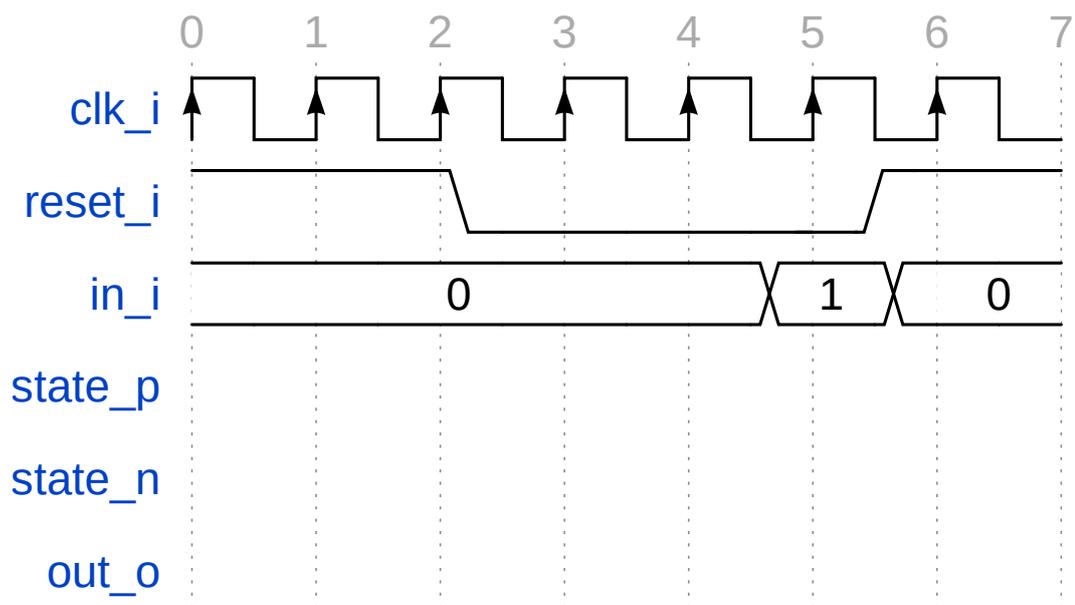
```

module state_machine(
  input logic clk_i,
  input logic reset_i,
  input logic in_i,
  output logic [1:0] out_o
);
  logic [1:0] state_p, state_n;

  always_ff @(posedge clk_i or posedge reset_i) begin
    if (reset_i) state_p <= 2'b00;
    else state_p <= state_n;
  end

  always_comb begin
    if (in_i == 0) state_n = state_p + 1;
    else state_n = state_p << 1;
  end
  // Output defined in truth table
endmodule

```



Q2. (10 points) **Memory and Cache:** Assume a directly-mapped data cache with a total size of 64 bytes, organized in 8 blocks, and 256 bytes of byte-addressable main memory. The latency for accessing the main memory is 200ns and the latency for accessing the cache is 20ns.

- (a) Why are caches used in modern processors, *i.e.*, what problem do they solve?
- (b) Name and explain the two types of locality that caches exploit.
- (c) Sketch the directly-mapped cache and explain how a cache access to the address 0x56 is performed. What checks are performed on which data and what are the expected values for a cache hit?
- (d) Assume the following piece of code being executed on a system. The local variables `i` and `sum2` are kept in registers. The data cache is empty at the beginning of the execution. What is the total latency for accessing *all* elements? For every access, state whether it is a cache hit H or miss M.

```
// Located at memory address 0x54
char array[4] = {1, 2, 3, 4};

int sum2 = 0;
for(int i = 0; i < 8; ++i)
    sum2 += array[i % 4]
```

Q3. (10 points) **Assembly:**

- (a) What is a calling convention and why is it needed? Explain what a calling convention covers.
- (b) Transform the following C-code to RISC-V assembly. All local variables of the C-code **must** be allocated on the stack. The global variable `g` is located at address `0xF00`. The RISC-V calling convention must be followed. The assembly startup code including the initialization of the stack is provided below. Write the assembly code for the two functions at the foreseen locations.

```
// Located at memory address 0xF00
int g;

int addglobal(int* p) {
    return *p + g;
}

int main() {
    int a = 3;
    g = 4;
    return addglobal(&a);
}
```

Assembly Reference

```
LW    rd,imm(rs1)
SW    rs1,imm(rs2)
ADD   rd,rs1,rs2
ADDI  rd,rs1,imm
SUB   rd,rs1,rs2
JAL   rd,imm
JALR  rd,imm(rs1)
```

```
_start:
    ADDI sp, zero, 0x700
    JAL ra, main
    EBREAK
```

```
main:
```

```
times3:
```

Q4. (10 points) **IPv6:**

- (a) List equivalent representations that shorten the address 2001:0fc7:0:0:2a1:0:0:0 after applying all possible rules for simplification.
- (b) How does Multicast work with IPv6?
- (c) What tasks are fulfilled by the Neighbor Discovery Protocol? Describe two **in detail**.

Q5. (10 points) **HTTP & DNS:**

- (a) Explain the new features introduced by HTTP/2.0. How is it different to previous HTTP versions?
- (b) Describe the properties of AJAX, Long Polling, and Web Sockets in relation to overhead and the possibility to push data to the client.
- (c) We usually rely on two types of DNS name servers. What is their purpose?