Computer Organization and Networks

(INB.06000UF, INB.07001UF)

Chapter 14: Wrap Up

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Stefan Mangard, www.iaik.tugraz.at

The Written Exams

- All written exams take 90 minutes
- Questions are in English
- You can write your answers in English or German

WRAP UP

Basics

(Chapters 1 – 3)

Topics

- Combinational logic
  - Logic gates, combinational circuits, synthesis
  - Truth table <-> Logic function <-> combinational circuit
- Numbers
  - Representations, arithmetic, positive/negative, comma
- Finite state machines
  - FSM/ASM graph <-> truth table <-> circuit
  - Next-state logic, output logic
  - Timing diagrams
  - Moore machine vs. Mealy machine

Processors, Part I

(Chapters 4 – 7)

Topics

- CPU & Memory
  - Von Neumann Model
  - Building blocks (Register file, ALU, Instruction Decoder, Control logic, RAM)
  - Main operations (Fetch, Decode, Execute)
  - ASM graphs of small CPUs (e.g. nano Risc-V)
  - Instruction Set (HW/SW Interface, types, examples, …)

- Software View
  - C <-> Assembler <-> Machine language
  - Stack
  - Subroutines
    - prolog, local variables, epilog, …
    - calling convention (Call by value, Call by reference, register usage & saving, …)

- Peripherals
  - Memory map
  - Polling
  - Bus protocol (synchronization)

Networks

(Chapters 8 – 11)

Topics

- Network Basics
  - OSI and TCP/IP Models
  - How to transfer data? -> Circuit vs Packet Switching
  - IEEE 802: Logical Link Control (LLC), Media Access Control (MAC)
  - Hubs and Switches (Forwarding / Filtering)

- (Between) Link & Network Layer
  - MAC vs IP Addresses -> ARP
  - IPv4 & ICMPv4: Subnets, MTU Path Discovery, NAT & Fragmentation
  - Multicasting & Routing

- Network & Transport Layer
  - IPv6 & ICMPv6: NDP (SLAAC, Router Discovery, …)
  - TCP & UDP: Flow & Congestion control, Sliding Window, Error handling

- Application Layer
  - HTTP: Versions, Request Types
  - Advanced Communication: AJAX, Long Polling, Web Sockets
  - DNS

Processors, Part II

(Chapters 12 – 13)

Topics

- Pipelining
  - Principle, typical stages and their functionality,
  - Handling control signals
  - Detection and handling of dependencies (forwarding, stalls, software, …)
  - Scoreboarding
  - HW/SW Contract
  - Techniques to a speed-up CPUs (overview)

- Caches
  - Principle and motivation
  - Concepts: directly mapped, set associative, set associative, tags, validity, cache sets, …
  - Handling of read (hit/miss, eviction, …)
  - Handling of write

- Interrupts
  - Principle and motivation
  - Interrupt service routine
  - Mapping interrupt sources to handling code in ISR