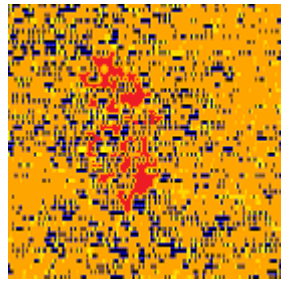
Power estimations / power simulations of VLSI designs



Motivation

In VLSI design, especially in case of low-power applications, the estimation of the power consumption of an implementation is an important step during the design phase. Such power estimations can be performed in different design phases, on different complexity / accuracy levels, and with different tools.

The goal of this project is to compare the results of different power estimation / power simulation methods (e.g. Encounter Power System, Modelsim, and RC-extracted simulation using Synopsys NanoSim) based on various existing implementations and/or newly implemented designs.

Project description

- Goals
  - Comparison of different power estimation / simulation methods regarding e.g. power values, runtime, accuracy.
- Tasks
  - Read into the topic of power estimation / power simulation
  - Get familiar with the IAIK design flow and the simulation software
  - Perform power estimations / power simulations of existing designs and/or a newly implemented (low power) design

Literature

- Encounter Power System
- Mentor Graphics Modelsim
- Synopsys NanoSim

Deliverables

- Project files (.zip, cleaned)
- Documentation (paper)
- Presentation (10 .ppt slides)

Project schedule

- Start: Immediately or in autumn
- Month 1: Study literature, play with IAIK design flow
- Month 2: Power estimate / simulate different designs; implement reference (low-power) designs
- Month 3: Final deliverables

Master Project

Studies: ☐ INF ☐ SEW ☑ TEL

Prerequisites

- Basic knowledge of VLSI design
- Interest in (low-power) hardware design

Advisor / contact

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