

Pipeline Controller Synthesis

Motivation

The control logic of a pipelined microprocessor is very hard to implement right, but rather easy to formally specify: An arbitrary program running on the pipelined processor should yield the same result as on a non-pipelined reference implementation. Therefore, such control logic is a perfect target for automated synthesis. We are currently implementing a tool that does that. In order to evaluate the approach, we need interesting benchmarks.

Project description

- Goals
 - Specifying a Burch-Dill style equivalence criterion for a pipelined microprocessor in SMTLIBv2 language
 - Evaluating and benchmarking the synthesis tool under development with the aforementioned benchmarks
- Tasks
 - Understand Theory
 - Pipeline equivalence
 - Controller synthesis
 - Specify
 - A new benchmark example
 - Extend current specification approach where necessary
 - Evaluate
 - Run benchmark on new tool

Literature

- Georg Hofferek, Roderick Bloem - "**Controller Synthesis for Pipelined Circuits Using Uninterpreted Functions**" - Ninth ACM/IEEE International Conference on Formal Methods and Models for Codesign (MemoCODE 2011)
- J. R. Burch and D. L. Dill - "**Automatic verification of pipelined microprocessor control**" - Sixth Conference on Computer Aided Verification (CAV'94), 1994. Springer LNCS 818.

Deliverables

- Specification of new benchmark example
- Documentation
- Presentation (15-20 min)

Project schedule

- Start Immediately
- Month 1 Understand theory and current state of the art
- Month 2 Create specification for new benchmark
- Month 3 Evaluate and refine benchmark

Master Project

Studies: INF SEW TEL Tech. Math.

Prerequisites

- Interest in formal methods and logic
- Basic knowledge about pipelined designs

Advisor / contact

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